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Collins Radio Company

Part 1

651S-1/1A General Purpose HF Receiver

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651S-1/1A General Purpose HF Receiver

COLLINS

description and principles of operation

Printed in USA

523-0764053-003218
3rd Edition, 15 October 1972

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NOTICE: **This section replaces second edition dated 1 May 1972.**

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description and principles of operation

1. GENERAL

The 651S-1/651S-1A (figure 1) is a triple-conversion superheterodyne receiver that provides 297,500 channels in the 250-kHz to 29.9999-MHz frequency range. It is a completely solid-state desk-top receiver and features direct-reading digital display of the operating frequency.

The standard operating modes of the 651S-1/1A are AM, SSB, and CW. Standard if filter bandwidths are 6 and 16 kHz, 2.7 kHz USB, and 2.7 kHz LSB.

Optional operating modes are narrow-band FM and ISB (independent sideband). Additional if filters are available and are described in paragraph 5. Including standard bandwidths, as many as eight if bandwidths are available. The optional operating modes and bandwidths require additional or different plug-in circuit cards for implementation.

Frequency coverage can be extended down to 12 kHz by use of an optional VLF converter. The vlf converter is part of special plug-in rf module (A6) that is used in place of the standard rf module normally supplied. In addition an optional frequency scan (automatic frequency scan) capability is available with the addition of a special card. The 651S-1/1A is capable of operation with narrow-band secure voice vocoder systems (NBSV) and radioteletypewriter systems (RTTY).

NOTE:
SILK-SCREEN ON BANDWIDTH SWITCH MAY VARY FOR THE DIFFERENCE PART NUMBERS OF THE 651S-1. THE APPEARANCE OF THE 651S-1A IS IDENTICAL TO THE 651S-1 EXCEPT FOR TYPE NUMBER AND AND SILK-SCREEN ON BANDWIDTH SWITCH.

TP3-0870-017

651S-1/1A General Purpose HF Receiver
Figure 1

All controls necessary for complete local operation are on the front panel of the receiver; however, remote control options are available. Two types of remote control are possible, Collins 3-pair serial digital control and teletypewriter-coded control.

To use Collins 3-pair serial digital control, the interconnect card must be removed and two cards added: the DCFE (device control functional element) card and the DCU (device control unit) card. With these cards installed, one or more receivers can be controlled by a digital processor such as the Collins 8311A-1 or 8311B-1.

To use Collins teletypewriter-coded control, the interconnect card must be removed and two cards added: the DCFE card and the TCU (teletypewriter control unit) card. With these cards installed, the 651S-1/1A can be remotely controlled using a Collins 514S-1 Remote Control Unit. Table 1 lists the 651S-1/1A configuration and the optional cards included in each configuration. Paragraph 5 describes the variations. A 115- or 230-Vac power cable is supplied with each configuration as required.

Table 2 lists external equipment required for a completely operable receiver and optional equipment available for special applications.

Table 3 lists the electrical and environmental characteristics and limitations of the 651S-1/1A.

2. PHYSICAL DESCRIPTION

The 651S-1/1A (figure 2) is a desk-top model receiver featuring completely solid-state design. A 19-inch speaker panel is available to rack mount the receiver (table 2). Refer to the installation section for mounting details. All the controls for manual operation are on the front panel and all points for external wiring/connections are on the rear panel, except the headset connection point on the lower front panel. Refer to the operation section for details.

The top-front panel is of black glass for good visibility of the electronic digital frequency display and the af/rf level meter.

The 651S-1/1A contains a sheet-metal chassis with removable module/card construction. A ventilated cover allows airflow into the bottom and out the back.

The circuit cards and the shielded rf module slide into a metal card cage. Space between the card cage and the dust cover allows air circulation. The 2-speed fan is thermostatically controlled.

The unit is 6.25 inches (15.9 cm) high (less mounting feet), 13.2 inches (33.5 cm) wide, 15.8 inches (40.1 cm) deep (less knobs), and weights 30.2 pounds (13.7 kg).

3. ELECTRICAL DESCRIPTION

The 651S-1/1A incorporates a unique method of tuning. It tunes in discrete 100-Hz steps: tuning information is derived from a 22-bit binary coded decimal (bcd) accumulator. Operating frequency is selected manually or by 3-pair digital remote control.

For manual tuning, three front-panel tuning knobs select the desired operating frequency in steps of 1 MHz, 0.1 MHz, and 100 Hz. These control switches drive the accumulator that consists of six up-down bcd counters.

In typical operation the 1-MHz and 0.1-MHz controls are used to enter the proper band and the 100-Hz control is used for fine tuning. The selected frequency information is applied to the frequency synthesizer cards and the numeric frequency display tubes.

The 100-Hz tuning control is an infrared photoelectric tuning switch that produces two square-wave outputs in quadrature when the shaft is turned. Card A14 determines the direction of rotation from these pulses and sends up or down pulses to the synthesizer. Two infrared emitters generate light that is interrupted by opaque lines screened on a transparent disc.

An optional keep-alive power circuit is available. In receivers that have this special circuit, a 6- to 8-Vdc battery can be connected to a terminal strip at the rear of the receiver. The battery will supply keep-alive power to frequency control card A14 so a temporary power loss will not cause a loss of frequency information.

Operation of the frequency circuits for remote control applications is the same as local control except for the method of driving frequency control card A14. Using 3-pair serial digital control, all functions and frequency selection can be controlled by a processor. Up to 30

Table 1. 651S-1/1A Configuration.

NOTES: 1. Power supply regulator card A1 (778-2949-001), synthesizer reference card A11 (793-9333-002), synthesizer mixer card A12 (793-9332-002), synthesizer vco card A13 (793-9331-003), and frequency control card A14 (783-9283-001) are used in all 651S-1/1A's.
2. Scan card 783-9368-001 is used in special applications of the 651S-1/1A.
3. Audio card *-003 is the current production model effectivity CI-72373.

TYPE	CONTROL TYPE	MODES/ BANDWIDTHS			OPT SQUELCH	OPT ISB	OPT VLF	FRONT PANEL COLOR	OPT IF FREQ	SUBASSEMBLY PN / 651S-1 PN 522-4836-	CHASSIS 606-9423-	AUDIO CARD A2 778-2948-	ISB CARD A3 778-2952-001	IF AMPLIFIER CARD A4 778-2951-	IF FILTER CARD A5A1 797-3571-	FILTER CARD A5A2 797-3585-	RF MODULE A6 790-1048-	DECODER/DRIVER CARD A7 778-2928-003	DECODER/DRIVER CARD A7 608-9087-001	DECODER/DRIVER CARD A7 608-9121-001	INTERCONNECT CARD A8 778-2924-	DCFE CARD A8 624-5744-001	DCU CARD A9 793-9414-001	DCU CARD A9 624-5781-001	DCU CARD A9 (HI-SPEED) 774-7842-001	TCU CARD A9 783-9480-001	SYNTHESIZER DIVIDER CARD A10 793-9334-
		STD	OPT AM	OPT CW																							
651S-1 -102 series (Cont)	Local control	16 kHz and 6 kHz AM; 2.7 kHz LSB; 2.7 kHz USB	3 kHz	1.1, 0.5, and 0.37 kHz	Squelch	No ISB	No vlf	Black	450 kHz if	004	005	002		001	001	010	008	X			006						002
					No squelch					104	003	003		001	001	002	008	X			006						002
			3 kHz	1.0, 3.0, and 0.2 kHz		ISB				110	003	003	X	001	001	003	008	X			004						002
						No ISB				111	003	003		001	001	003	008	X			004						002
					Squelch					121	005	002		001	001	003	008	X			004						002
						ISB				122	005	002	X	001	001	003	008	X			004						002
				0.5 kHz	No squelch		Vlf			106	003	003	X	001	001		008	X			004						002
						No ISB				102	003	003		001	001		008	X			004						002
					Squelch		No vlf			120	003	003		001	001		010	X			004						006
								Gray		124	005	002		001	001		008	X			004						002
					No squelch					126	003	003		001	001		008	X			004						002
			3 kHz	0.320, 1.1 and 3 kHz				Black		134	003	003		001	001	010	008	X			004						002
				0.2, 0.5, 1.0 and 3 kHz			Vlf			132	003	003		001	001	003	010	X			004						006
						ISB				133	003	003	X	001	001	003	010	X			004						006
				4.0, 2.0, and 1.1 kHz		No ISB			455.5 kHz	128	003	005		001	007	011	008	X				X		X			002
	Processor control			1.0, 3.0, and 0.2 kHz						107	003	003		001	001	003	008	X				X	X				002
						ISB	No vlf			108	003	003	X	001	001	003	008	X				X	X				002
										113	006	003		003	001	003	008	X				X	X				002
				0.5 kHz	Squelch				450 kHz if	125	005	002		001	001		008	X				X	X				002
					No squelch	No ISB				103	003	003		001	001		008	X				X	X				002
			3 kHz	0.5, 1.1 and 3 kHz						129	003	003		001	001	012	008	X				X	X				002

Table 1. 651S-1/1A Configuration (Cont).

NOTES: 1. Power supply regulator card A1 (778-2949-001), synthesizer reference card A11 (793-9333-002), synthesizer mixer card A12 (793-9332-002), synthesizer vco card A13 (793-9331-003), and frequency control card A14 (783-9283-001) are used in all 651S-1/1A's.
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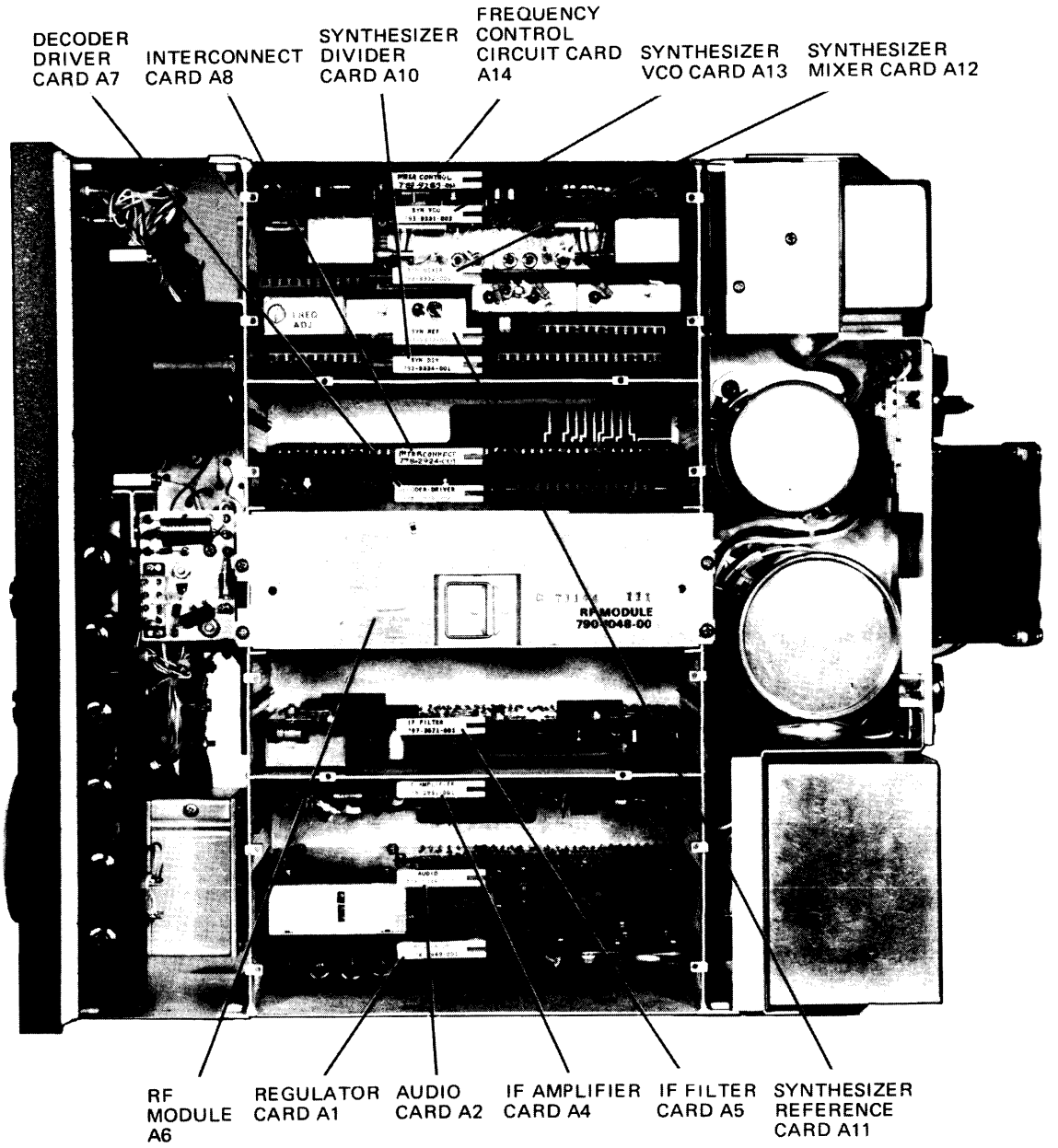
		STD	OPT AM	OPT CW																							
651S-1 -102 series (Cont)	Processor control	16 kHz and 6 kHz AM; 2.7 kHz LSB; 2.7 kHz USB	3 kHz	0.2, 0.5, 1.0, and 3 kHz	Squelch	ISB	No vlf		450 kHz if	131	005	002	X	001	001	003	008	X				X					002
							Vlf			135	005	002	X	001	001	003	010	X				X					006
	Teletypewriter control			0.5 kHz		No ISB				123	003	003		001	001		008	X				X				X	002
651S-1 -152 series	Local control				No squelch	No ISB	No vlf	Black	455.0 kHz if	152	007	*003		004	010		020		X		004						002
						ISB				156	007	*003	X	004	010		020		X		004						002
			3 kHz	0.370, 0.5, 1.1 and 3 kHz		No ISB				154	007	*003		004	012	010	020		X		006						002
				0.5, 1.1, and 3 kHz		ISB				180	007	*003		004	011	012	020		X		007						002
										181	007	*003	X	004	011	012	020		X		007						002
							Vlf			182	007	*003		004	011	012	021		X		007						006
	Processor control									153	007	*003		004	010		020		X			X		X			002
										179	007	*003		004	010				X			X			X		002
			3 kHz	0.2, 0.5, and 3 kHz		No ISB	No vlf			183	006	*003		003	011	003	020			X		X		X			002
				1, 2, 3, and 4 kHz					455.5 kHz if	184	009	005		003	007	011	020		X			X		X			002
	Teletypewriter control								455.0 kHz if	173	007	*003		004	010		020		X			X				X	002
651S-1A	Local control		3 kHz	1.1, 0.5, and 0.37 kHz	Squelch					622-1062-001	005	004		004	006	010	020			X	006						002



Subassembly Location
Figure 2

Table 2. Required or Optional Equipment.

ITEM	USE	RECOMMENDED TYPE
Headset or Speaker } Required for a completely operable receiver	Audio output.	Headset: Collins HS-1 600 ohms unbalanced, 3 watts minimum or equivalent Speaker: 8 ohms, 4 watts capability
4800-bit/s serial digital remote control	Optional remote operation.	Collins 8311A-1 or 8311B-1 Device Control Computer system
Mount/speaker panel	Rack mount/audio output.	Collins 699J-1 Speaker Panel
Teletypewriter-coded control	Optional remote operation.	Collins 514S-1 Remote Control Unit
Auto scan control panel	Optional remote frequency scan operation.	Auto scan control panel, Collins pn 620-9030-001
Auto scan control	Optional frequency scan operation.	Collins pn 609-1565-001
Modification kit		
Plate, switch	Installed over REMOTE CONTROL switch on front panel.	Collins pn 609-0944-001
Adapter card	Installed in place of auto scan card to permit normal operation without restrapping the 651S-1/1A sideboard.	Collins pn 609-1554-001
*Auto scan control card	Provides automatic scanning of preset receiver frequencies.	Collins pn 783-9368-001
*Also available as an end item.		

receivers can be controlled by one processor. To use 3-pair digital control, the DCFE card is mounted in place of interconnect card A8 and DCU card A9 is added. Three twisted pairs of input wires provide the interface between the receiver and the remote control processor. All information is fed to the optional DCU and DCFE cards that override all manual controls (except audio gain) and automatically set up the 651S-1/1A for operation. The input is a 32-bit control word on a 4800-Hz or 76.8-kHz (for hi-speed DCU) biphase modulated format. The DCU must be strapped for proper addressing (refer to paragraph 4.1 of the operation section for details).

For 514S-1 remote control operation, the DCFE card is mounted in place of interconnect card A8 and TCU card A9 is added. Three pairs of input wires provide the interface between the receiver and the 514S-1. One pair of wires is for the audio lines; the other two pairs are for standard 20-mA teletypewriter loops. External jumpers may be used to wire the system for a single teletypewriter loop. Up to 15 receivers can be controlled by strapping 4 wires on the TCU for proper addressing (refer to the operation section paragraph 4.2 for details).

Independent sideband (ISB) operation is optional on the 651S-1/1A. ISB if amplifier card A3 is required for this option. In ISB operation, both USB and LSB filtering circuits are enabled and the stronger of the USB and LSB signals controls the rf AGC level for the front end of the receiver. Separate audio and if output points are on the rear chassis for ISB signals.

To obtain frequency scanning capability, auto scan card A9 (783-9368-001) is available. This card contains all the required circuits to provide frequency scan operation.

Table 3. Equipment Specifications.

CHARACTERISTIC	LIMITATIONS
	Note All voltages are "hard" volts, that is, open circuit voltage from 50-ohm resistive source, unless otherwise specified.
Frequency range	250 kHz to 29.9999 MHz; 12 kHz to 29.9999 MHz optional.
Frequency control	Phase locked in 100-Hz steps. Provisions for interpolation in 10-Hz steps.
Frequency stability	5 parts in 10^7 total.
Frequency adjustment	1-MHz and 0.1-MHz steps by rotary switches. 100-Hz steps by continuous tuning control. May be controlled remotely by Collins 3-pair serial digital method (optional) or by Collins 514S-1 Remote Control Unit.
Frequency readout	7-bar segment tubes, six places.
Modes	
Standard	AM, SSB, and CW.
Optional	Narrow-band FM, ISB (independent sideband)
Bandwidth	PASSBAND (3 dB) — REMARKS
Standard	16 kHz (nominal) — AM 6 kHz (-6 dB) — AM 2.7 kHz — LSB 2.7 kHz — USB
Optional	0.2 kHz — Increased selectivity for CW 0.370 kHz — Center frequency ±2 kHz, suitable for RTTY. 0.5 kHz — Increased selectivity for CW. 1.0 kHz — CW. 3.0 kHz — Suitable for narrow-band AM. 1.1 kHz — Center frequency +2 kHz suitable for RTTY. 2.0 kHz — Increased selectivity for CW. 4.0 kHz — Increased selectivity for CW.
Sensitivity for 10-dB signal-to-noise ratio	
0.250 to 0.4 MHz	SSB: 5 μV (2.7 kHz bandwidth) AM: 35 μV (6 kHz bandwidth)
0.4 to 1.999 MHz	SSB: 2.5 μV (2.7 kHz bandwidth) AM: 10 μV (6 kHz bandwidth)
2.0 to 29.9999 MHz	SSB: 0.7 μV (2.7 kHz bandwidth) AM: 3.5 μV (6 kHz bandwidth) NBFM: 1 μV (12 dB SINAD)
(Cont)	

Table 3. Equipment Specifications (Cont).

CHARACTERISTIC	LIMITATIONS
Sensitivity for 10-dB signal-to-noise ratio (Cont)	
12 to 559.9 kHz (50-ohm input) (with optional vlf converter)	SSB: 2.5 μV (2.7 kHz bandwidth) AM: 12 μV (6 kHz bandwidth)
Gain	In SSB, 3 μV produces 0.5 W of audio into 8-ohm load or 1 mW (0 dBm) into 600-ohm line output.
Audio output power	2 W into 8-ohm load at speaker terminal, with not more than 3% total distortion, 5-mW peak (+7 dBm), at 600-ohm line output with not more than 1% total distortion.
Audio output impedance	8 ohms nominal at speaker terminal, 600 ohms nominal at headphone jack. 600 ohms on line audio outputs, balanced, center tapped.
Audio response (600-ohm line audio)	With 1 dB from 100 Hz to 4 kHz. (If filter response will further modify overall receiver response; for example, 2.7-kHz SSB filter response is -3 dB from 350 Hz to 3050 Hz.)
If output	50 mV at 450-kHz, 50-ohm load. Same for the ISB channel.
Audio hum and noise	At least 40 dB below maximum output.
Antenna input impedance	50 ohms nominal unbalanced.
Automatic gain control	
Audio rise	No more than 6 dB for input signal of 3 μV to 0.3 V.
Release time	100 ms or 1 s, switchable. AGC can be disabled.
Cross modulation (-10 dB, 30% modulation with 50 μV desired signal)	±50 kHz from operating frequency, 0.35 V; ±10% from operating frequency, 0.50 V.
Spurious response, internal	Not more than 2 μV (except at 0.9, 9.9, 19.8, and 20.7 MHz not more than 10 μV).
Squelch (optional)	Adjustable squelch.
Bfo	Fixed 450 kHz bfo; derived from reference oscillator of synthesizer. Variable 450-kHz bfo may be tuned ±900 Hz in CW mode. SSB mode bfo tunes ±60 Hz in 10-Hz steps to interpolate between 100-Hz positions.
Antenna input protection	Overload diodes provide protection against strong signals up to 10 volts rms.
Metering	Front panel meter measures rf signal level in decibels above 1-μV input signal, or 600-ohm audio line level in dBm.
MTBF	3,000-h field operation.
Mounting	19-in (48.3 cm) rack panel kit or table top.

Table 3. Equipment Specifications (Cont).

CHARACTERISTIC	LIMITATIONS
Temperature	0 °C to +55 °C (+32 °F to +131 °F).
Humidity	90%.
Altitude	9144 m (30,000 ft).
Power requirements	115/230 V ±10%, 47 to 63 Hz, 70 W. An additional 40 W may be required to power optional circuits. Optional external battery for keep-alive function, +6 to +8 V, 1 A.

To obtain the optional if filter bandwidths, filter FL1 (mounts on if filter card A5A1) and/or subcard A5A2 (mounts on if filter card A5A1) is available. This subcard contains the additional desired optional filters.

4. PRINCIPLES OF OPERATION

4.1 Overall Operation

4.1.1 Signal Operation, Standard Configuration (Refer to figure 3.)

The received signal is routed through a 30-MHz low-pass filter that attenuates images and spurious responses. The signal is then applied through one of the diode-switched bandpass filters, depending on the operating frequency and rf module A6 being used. On Collins part numbers 790-1048-008/-010, there are 10 band-pass filters: the filter ranges are 0 to 0.5599 MHz, 0.56 to 1.9999 MHz, 2.0 to 2.9999 MHz, 3.0 to 3.9999 MHz, 4.0 to 5.9999 MHz, 6.0 to 7.9999 MHz, 8.0 to 11.9999 MHz, 12.0 to 15.9999 MHz, 16.0 to 23.9999 MHz, or 24.0 to 29.9999 MHz. On Collins part number 790-1048-020/-021, there are three bandpass filters: 0 to 0.5599 MHz, 0.56 to 1.9999 MHz, or 2.0 to 29.9999 MHz.

After proper bandpass filtering, the received signal is mixed with variable injection of from 79.3501 to 109.10 MHz to produce 109.35 MHz. This signal is applied through a 109.35-MHz crystal filter with 16-kHz bandwidth to a second mixer. At this stage the 109.35-MHz signal is mixed with a 99-MHz injection signal to produce 10.35 MHz. This signal is amplified and applied through either an 8-dB pad or one of three 10.35-MHz crystal filters. The crystal filters (various bandwidths) are used in cascade with mechanical filters to provide selectivity and good signal-to-noise ratio for various bandpass options of CW and AM operation. When 16-kHz bandwidth is desired, the 8-dB pad is inserted to maintain a nominal signal level.

The 10.35-MHz signal is mixed with 9.9 MHz to produce 450 kHz. It is then applied through one of three 450-kHz mechanical filters (USB, LSB, or AM) or a crystal filter (narrow-band CW mode), or the filters are bypassed (when 16-kHz bandwidth is desired). The inputs and outputs to and from the filters are FET switched.

The 450-kHz signal then goes through several stages of if amplification and if AGC is applied at these points to control the receiver gain. The signal path branches after three stages; part goes to an if output strip, part is used for SSB audio detection, part is used for AM and AGC detection, and part is used for FM detection.

The if output portion goes through three more stages of amplification and is applied to a rear connector for monitoring.

The signal portion for SSB product detection is amplified one more time to complete the step-up in the if strip. This output is applied with the bfo signal to a dual-gate FET to produce SSB audio. The signal portion for AM audio and AGC is applied to a 2-stage AGC amplifier. Its output is transformed and then demodulated by an emitter follower and used as AM audio and AGC. The FM signal is picked off at a high-level point in the 2-stage AGC amplifier and applied to an FM limiter/discriminator circuit.

All the audio signals are applied to the audio amplifier card. Specific enabling gate signals determine which mode audio signal is to be amplified; that is, AM enable, CW enable, etc. The audio is amplified in several stages and the

5-mW output from a 600-ohm transformer output is applied to a rear chassis terminal strip for external power amplification. Audio is also applied through the front panel volume control to a power amplifier circuit. This audio signal is amplified to provide a 20-W average into an 8-ohm speaker, and to provide an audio output for headphones.

Also contained on the audio card are variable bfo circuits and optionally, audio squelch circuit.

4.1.2 Signal Operation, Optional Configurations (Refer to figure 3.)

4.1.2.1 ISB

An optional card, 450-kHz independent sideband (ISB) if module A3, is available for ISB operation. With this card inserted and ISB mode selected, USB and LSB signals are simultaneously received and processed by the 651S-1.

Any signals passing through the LSB mechanical filter are switched by the FET filter output gates to ISB if module A3. Signals passing through the USB mechanical filter are routed through the regular if amplifier module, as in normal operation.

The ISB AGC amplifier develops an rf AGC voltage that is applied, along with another rf AGC voltage developed by the normal if/rf AGC detector, to the 109.35-MHz mixer and to the 10.35-MHz if amplifier. These two rf AGC signals represent the relative strengths of the USB and LSB signals. The rf AGC produced by the stronger signal predominates and automatically adjusts the receiver circuits for both USB and LSB reception. The ISB card provides the audio output for LSB signals. The USB audio signals are provided by the standard receiver circuits (refer to paragraph 4.1.1 for normal operation).

4.1.2.2 VLF

Two subassemblies are replaced to obtain vlf coverage: rf module A6 and synthesizer divider card A10. Table 1 lists these unique cards.

The rf module for vlf has an up-converter and filter circuit that mixes 9.9 MHz with the incoming vlf signal to produce 9.912 to 10.4599 MHz. This is then applied to the main 109.35-MHz mixer. All signals below 560 kHz will be processed by the up-converter.

The synthesizer divider card for vlf operation has vlf-enable and combinational logic circuits that cause injection frequencies 9.9 MHz above the incoming signals to be produced for signals below 560 kHz.

4.1.2.3 Automatic Frequency Scan Operation

An optional card, auto scan control card A9, is available for automatic frequency scan operation. With this card inserted, two jumper straps removed from the 651S-1 chassis sideboard (refer to installation section), and the receiver placed in the REMOTE mode, frequency scan coverage up to 100 kHz from an initial receiver frequency is provided. Scanning of the receiver frequency is conducted upward (higher in frequency) from the initial starting point. When the upper limit is reached, the receiver automatically returns (scans down) to the lower limit and repeats an upward scan.

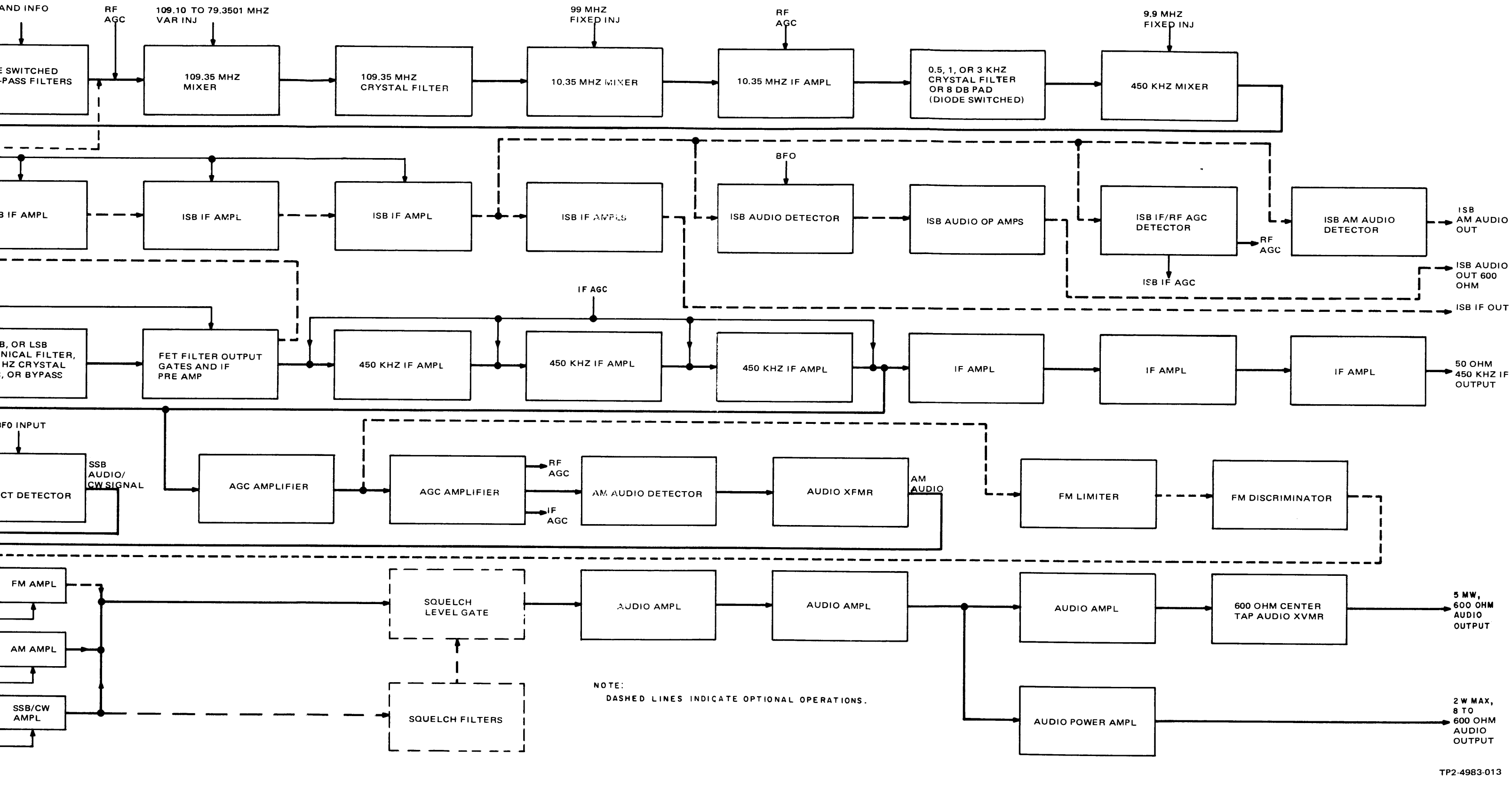
The frequency scanning steps will be in 100-Hz increments, compatible with the frequency synthesizer circuits in the receiver.

The frequency scan limits (range) are programmable internally (on-card strapping) in 100-Hz increments or externally in 1-kHz increments by using auto scan control panel, Collins part number 620-9030-001, interfaced through connector J62 at the rear of the receiver.

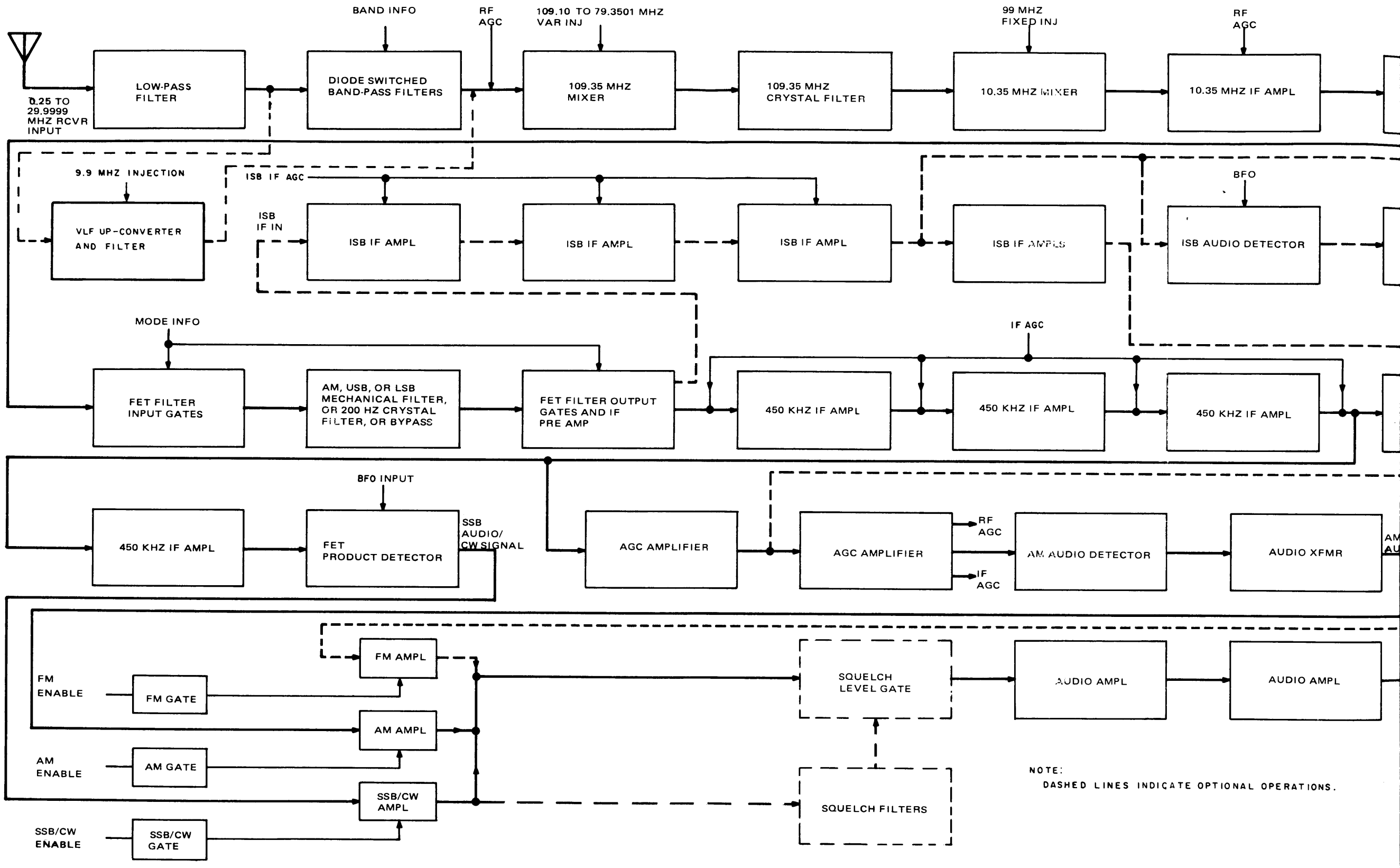
The dwell time (period in which the receiver remains on a discrete frequency) is programmable internally (on card strapping) in 100-millisecond increments from 100 to 600 miliseconds, or externally in 100-millisecond increments from 200 to 600 milliseconds using the auto scan control panel.

Frequency scan time (scan-up or scan-down) depends upon the frequency scan range and dwell time programmed. Scan-up shall not exceed 10 minutes and scan-down shall not exceed 5 seconds.

For card installation and strapping information, refer to the installation section.



Signal Operation, Functional Diagram Control
Figure 3


0.25 TO 29.9999 MHZ RCVR INPUT
LOW-PASS FILTER
BAND INFO
RF AGC
DIODE SWITCHED BAND-PASS FILTERS
109.10 TO 79.3501 MHZ VAR INJ
109.35 MHZ MIXER
109.35 MHZ CRYSTAL FILTER
99 MHZ FIXED INJ
10.35 MHZ MIXER
RF AGC
10.35 MHZ IF AMPL
9.9 MHZ INJECTION
VLF UP-CONVERTER AND FILTER
ISB IF AGC
ISB IF IN
ISB IF AMPL
ISB IF AMPL
ISB IF AMPL
ISB IF AMPLS
BFO
ISB AUDIO DETECTOR
MODE INFO
FET FILTER INPUT GATES
AM, USB, OR LSB MECHANICAL FILTER, OR 200 HZ CRYSTAL FILTER, OR BYPASS
FET FILTER OUTPUT GATES AND IF PRE AMP
IF AGC
450 KHZ IF AMPL
450 KHZ IF AMPL
450 KHZ IF AMPL
BFO INPUT
450 KHZ IF AMPL
FET PRODUCT DETECTOR
SSB AUDIO/ CW SIGNAL
AGC AMPLIFIER
AGC AMPLIFIER
RF AGC
IF AGC
AM AUDIO DETECTOR
AUDIO XFMR
FM AMPL
FM ENABLE
FM GATE
AM AMPL
AM ENABLE
AM GATE
SSB/CW AMPL
SSB/CW ENABLE
SSB/CW GATE
SQUELCH LEVEL GATE
SQUELCH FILTERS
AUDIO AMPL
AUDIO AMPL
NOTE:
DASHED LINES INDICATE OPTIONAL OPERATIONS.

4.1.3 Control Circuits, Local Operation (Refer to figure 4.)

In local operation, frequency selection, mode selection, and gain control are provided by the selector switches on the front panel of the receiver. Frequency information from the variable drum switch (100-Hz steps), the 0.1-MHz step selector, and the 1-MHz step selector, is applied to up-down counter circuits on frequency control card A14. The up-down counters provide parallel bcd frequency information to decoder/driver card A7, synthesizer divider card A10, and to the bcd to 7-bar decoder/drivers on card A14.

Decoder/driver card A7 uses the bcd frequency information from A14 to develop frequency band information that is routed to rf card A6. This band information is used by A6 to enable the proper bandpass filter on card A6.

The bcd to 7-bar decoder/drivers on card A14 decode the frequency information from the up-down counters and use this decoded frequency data to control the 7-bar numeric readout tubes on the front panel of the receiver.

The synthesizer circuits (made up of synthesizer divider card A10, synthesizer reference card A11, synthesizer mixer card A12, and synthesizer vco card A13) use the bcd frequency information from card A14 to develop the variable injection frequency that is applied to rf card A6. The synthesizer circuits also apply a fixed injection frequency to rf card A6, an if injection signal to if filter card A5, and the fixed bfo signal to if amplifier card A4.

The mode and gain information from the front-panel controls is applied to interconnect card A8. Card A8 routes this information to the applicable if and af cards.

4.1.4 Control Circuits, Remote Operation (Refer to figure 4.)

In remote operation, decoder/driver card A7, the bcd to 7-bar decoder/driver circuits on frequency control card A14, and the synthesizer circuits perform the same functions as in local operation. Interconnect card A8, however, is replaced by optional DCFE card A8, and optional DCU card A9 is added so the receiver can be controlled by an external serial digital control device. Optional DCFE card A8 and TCU card A9 are required so the receiver can be controlled by a 514S-1 Remote Control Unit.

DCU card A9 receives properly addressed biphase modulated sine-wave control data from the external digital control device. This control information appears on the control bus to the DCU, is converted by the DCU to digital control data, and is routed by the DCU to optional DCFE card A8. DCFE card A8 develops bcd frequency information and distributes this data to decoder/driver card A7, to the bcd to 7-bar decoder/drivers on card A14, and to the synthesizer circuits. The frequency information is then processed as in local operation (refer to paragraph 4.1.3).

Mode and gain control data (except audio gain) also appear on the control bus and are routed through DCU card A9 to DCFE card A8. The DCFE then sends this control data to the af and if cards as necessary to obtain the desired mode or gain level. Audio gain is controlled manually, as in local operation.

Monitor data is sent from the rest of the receiver circuits to DCFE card A8 in the form of digital monitor data. The DCFE routes this monitor data to DCU card A9 where it is converted to biphase modulated sine-wave data and sent to the external control device. This monitor data informs the control device that the receiver responded properly to the control information. The monitor data also indicates fault in the receiver circuits.

TCU card A9 receives properly addressed teletypewriter-coded control data from a 514S-1 Remote Control Unit. The control data is decoded and converted by the TCU to digital control data, and is routed to the optional DCFE card A8. The DCFE operates in the same manner as previously described, with the DCU. The TCU receives monitor data from the DCFE, encodes it into teletypewriter code, and transmits it to the 514S-1.

4.1.5 Frequency Synthesizer Circuits, Operation (Refer to figure 5.)

The 651S-1/1A frequency generating circuits provide all the injection frequencies required to select any 1 of 297,500 channels over the 0.25- to 29.9999-MHz tuning range in 100-Hz intervals. The outputs are selected and controlled by the operating frequency selected.

The synthesizer circuits are divided into two functional groups, the reference group and the frequency stabilizer group. The reference group consists of the 9.9-MHz frequency standard and the reference multipliers/dividers and produces the fixed injection signals. The frequency stabilizer group consists of phase-lock loops 1 and 2 and produces the variable rf injection signal.

The reference group generates all the reference signals required by the synthesizer circuits themselves, as well as the 450-kHz fixed bfo and 9.9-MHz if injection signals and the 99-MHz rf injection signals. The outputs from the reference group are all derived from the 9.9-MHz frequency standard. The 9.9-MHz standard signal is applied to the multipliers and dividers that provide the proper multiplication and division ratios to produce the required outputs.

The 9.9-MHz standard signal is multiplied by 10 to produce the 99-MHz injection output and divided by 22 to produce the 450-kHz injection signal. The standard signal is divided by 990 to produce the 10-kHz reference signal for phase-lock loop 2 and is divided by 1000 to produce the 9.9-kHz reference signal for phase-lock loop 1. All of the outputs from the reference group are coherent (in fixed phase relationship) with the 9.9-MHz standard signal.

The frequency group generates any one of 297.500 discrete injection frequencies at 100-Hz intervals from 79.3501 to 109.100 MHz. The 297.500 injection signals correspond to the 297.500 operating channels over the 0.25- to 29.9999-MHz tuning range of the receiver. These injection signals are selected by the bcd frequency codes applied to the two phase-lock loops by frequency control card A14 (or by optional DCFE card A8 in remote control).

The applied bcd codes control the division ratio of each loop. Operating channel frequencies and the corresponding bcd frequency codes, loop division ratios, and loop frequencies are summarized in table 4.

The first column in table 4 indicates the channel and the next six columns show the bcd frequency codes for each digit of the channel frequency. The last four columns show the corresponding division ratios and output frequencies of the two phase-lock loops. The channel frequency is changed in 100-Hz or 1-kHz steps by simultaneously changing the division ratios (N_1 and N_2) of the two phase-lock loops.

For 100-Hz steps, N_1 and N_2 are changed by a factor of 1, and for 1-kHz steps, by a factor of 10. This relationship is shown for the 2.0000- to 2.0090-MHz frequency range in the table. For 10-kHz, 100-kHz, 1-MHz, or 10-MHz steps, only N_2 is changed by 1, 10, 100, or 1000 while N_1 remains constant.

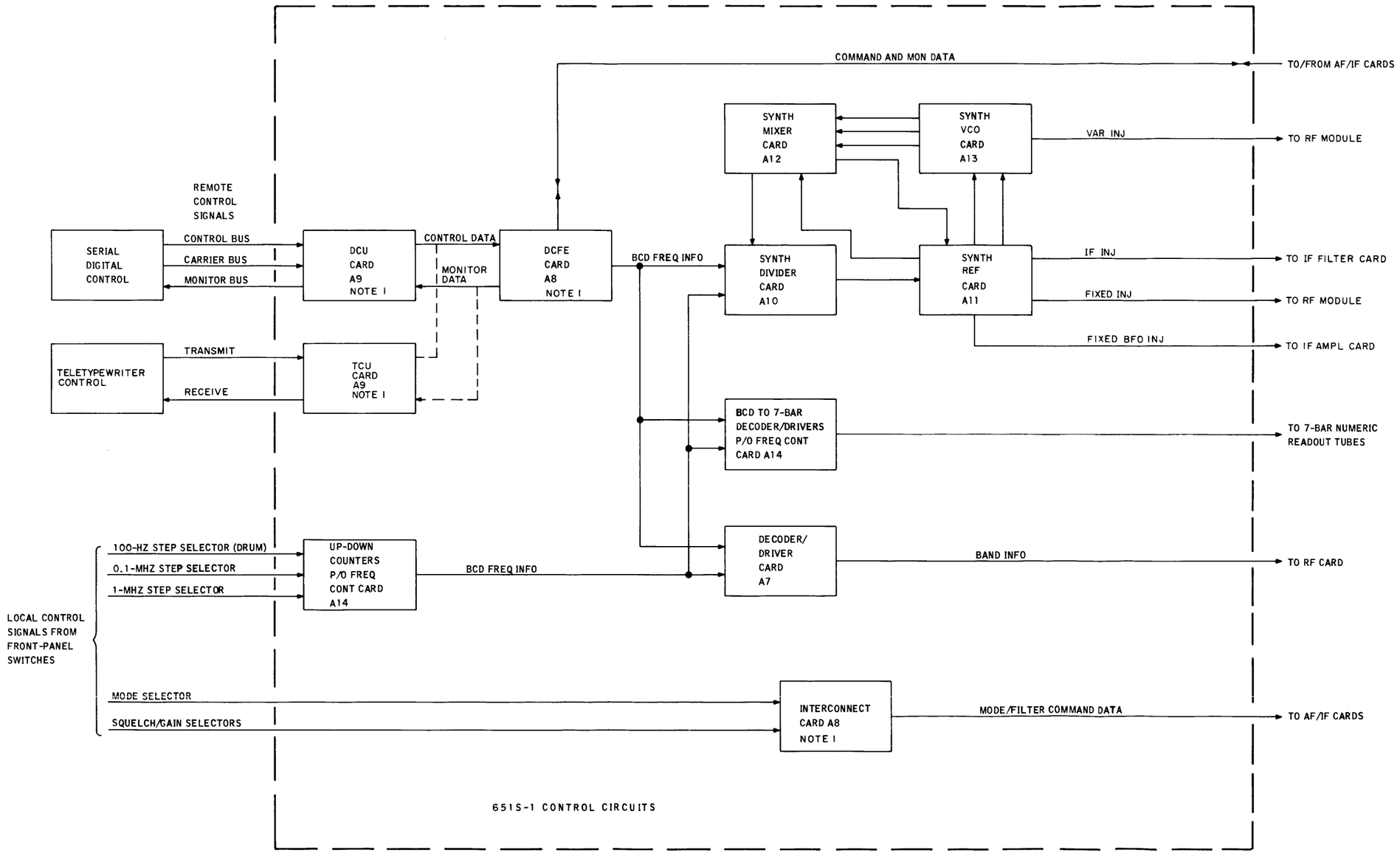
When the two least significant digits of the channel frequency reach 99 and then advance to 100, division ratio N_1 is reset to 1400 and N_2 is reset to the division ratio required for the selected channel frequency. This relationship is shown for the 2.0099-MHz channel in the table.

The variable injection output frequency (f_0) may be expressed as a function of loop frequencies and division ratios in the following equation:

$$f_0 \text{ (MHz)} = 99 + N_1 (9.9 \times 10^{-3}) - N_2 (10 \times 10^{-3})$$

The relationship of the variable injection to the corresponding channel frequency is established as the difference between the 109.3500-MHz signal developed in the associated receiver circuits and the variable injection frequency. For example, if the variable injection frequency is 107.3400 MHz, the corresponding channel is 2.0100 MHz. This relationship may be verified by referring to table 4.

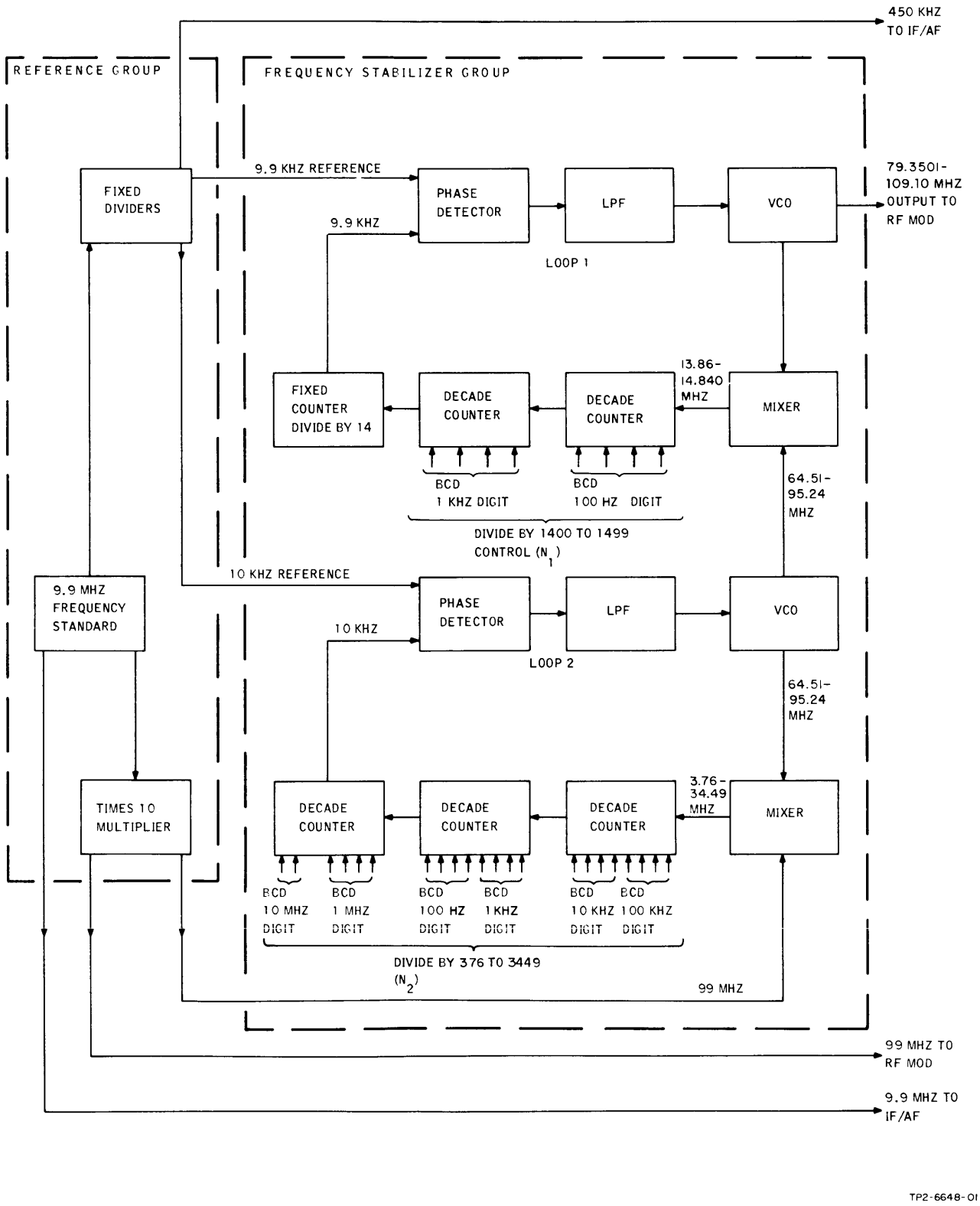
If the vlf option is installed, the synthesizer divider card (CPN 793-9334-006) for vlf replaces the normal divider card. No new mixing injection signals are generated; however, logic circuits are included that control the frequency of the mixing signals when vlf is enabled. These logic circuits command the variable injection synthesizers to produce injection frequencies for signals that are actually 9.9 MHz higher than the actual incoming signal. This is because 9.9 MHz fixed injection is added to all incoming signals below 560 kHz. For example, if 12 kHz is the incoming frequency, the synthesizer is directed to act as if 9.912 MHz were received, and so on up to 560 kHz.



NOTE:
1. IN REMOTE CONTROL OPERATION, DCFE CARD A8 REPLACES INTERCONNECT CARD A8 AND DCU OR TCU CARD A9 IS INSTALLED.
IN LOCAL CONTROL OPERATION, INTERCONNECT CARD A8 REPLACES DCFE CARD A8 AND DCU OR TCU CARD IS REMOVED.

TP2-6548-014

Control Circuits, Functional Diagram
Figure 4



Frequency Synthesizer Circuit, Functional Diagram
Figure 5

Table 4. Stabilizer Frequency Chart.

CHANNEL (MHz)	BCD FREQUENCY CODES						PHASE-LOCK LOOP 2		PHASE-LOCK LOOP 1	
	10-MHz DIGIT	1-MHz DIGIT	100-kHz DIGIT	10-kHz DIGIT	1-kHz DIGIT	100-Hz DIGIT	DIVISION RATIO (N_2)	OUTPUT FREQ (MHz)	DIVISION RATIO (N_1)	OUTPUT FREQ (f_o)(MHz)
00.2500	00	0000	0010	0101	0000	0000	376	95.24	1400	109.1000
00.4000	00	0000	0100	0000	0000	0000	391	95.09	1400	108.9500
00.5000	00	0000	0101	0000	0000	0000	401	94.99	1400	108.8500
00.6000	00	0000	0110	0000	0000	0000	411	94.89	1400	108.7500
00.7000	00	0000	0111	0000	0000	0000	421	94.79	1400	108.6500
00.8000	00	0000	1000	0000	0000	0000	431	94.69	1400	108.5500
00.9000	00	0000	1001	0000	0000	0000	441	94.59	1400	108.4500
01.0000	00	0001	0000	0000	0000	0000	451	94.49	1400	108.3500
02.0000	00	0010	0000	0000	0000	0000	551	93.49	1400	107.3500
02.0001	00	0010	0000	0000	0000	0001	552	93.48	1401	107.3499
02.0002	00	0010	0000	0000	0000	0010	553	93.47	1402	107.3498
02.0003	00	0010	0000	0000	0000	0011	554	93.46	1403	107.3497
02.0004	00	0010	0000	0000	0000	0100	555	93.45	1404	107.3496
02.0005	00	0010	0000	0000	0000	0101	556	93.44	1405	107.3495
02.0006	00	0010	0000	0000	0000	0110	557	93.43	1406	107.3494
02.0007	00	0010	0000	0000	0000	0111	558	93.42	1407	107.3493
02.0008	00	0010	0000	0000	0000	1000	559	93.41	1408	107.3492
02.0009	00	0010	0000	0000	0000	1001	560	93.40	1409	107.3491
02.0010	00	0010	0000	0000	0001	0000	561	93.39	1410	107.3490
02.0020	00	0010	0000	0000	0010	0000	571	93.29	1420	107.3480
02.0030	00	0010	0000	0000	0011	0000	581	93.19	1430	107.3470
02.0040	00	0010	0000	0000	0100	0000	591	93.09	1440	107.3460
02.0050	00	0010	0000	0000	0101	0000	601	92.99	1450	107.3450
02.0060	00	0010	0000	0000	0110	0000	611	92.89	1460	107.3440
02.0070	00	0010	0000	0000	0111	0000	621	92.79	1470	107.3430
02.0080	00	0010	0000	0000	1000	0000	631	92.69	1480	107.3420
02.0090	00	0010	0000	0000	1001	0000	641	92.59	1490	107.3410
02.0099	00	0010	0000	0000	1001	1001	650	92.50	1499	107.3401
02.0100	00	0010	0000	0001	0000	0000	552	93.48	1400	107.3400
02.0200	00	0010	0000	0010	0000	0000	553	93.47	1400	107.3300
02.0300	00	0010	0000	0011	0000	0000	554	93.46	1400	107.3200
02.0400	00	0010	0000	0100	0000	0000	555	93.45	1400	107.3100
02.0500	00	0010	0000	0101	0000	0000	556	93.44	1400	107.3000
02.0600	00	0010	0000	0110	0000	0000	557	93.43	1400	107.2900
02.0700	00	0010	0000	0111	0000	0000	558	93.42	1400	107.2800
02.0800	00	0010	0000	1000	0000	0000	559	93.41	1400	107.2700
02.0900	00	0010	0000	1001	0000	0000	560	93.40	1400	107.2600
02.1000	00	0010	0001	0000	0000	0000	561	93.39	1400	107.2500
02.2000	00	0010	0010	0000	0000	0000	571	93.29	1400	107.1500
02.3000	00	0010	0011	0000	0000	0000	581	93.19	1400	107.0500
02.4000	00	0010	0100	0000	0000	0000	591	93.09	1400	106.9500
02.5000	00	0010	0101	0000	0000	0000	601	92.99	1400	106.8500
02.6000	00	0010	0110	0000	0000	0000	611	92.89	1400	106.7500
02.7000	00	0010	0111	0000	0000	0000	621	92.79	1400	106.6500
02.8000	00	0010	1000	0000	0000	0000	631	92.69	1400	106.5500
02.9000	00	0010	1001	0000	0000	0000	641	92.59	1400	106.4500
03.0000	00	0011	0000	0000	0000	0000	651	92.49	1400	106.3500
04.0000	00	0100	0000	0000	0000	0000	751	91.49	1400	105.3500
05.0000	00	0101	0000	0000	0000	0000	851	90.49	1400	104.3500
06.0000	00	0110	0000	0000	0000	0000	951	89.49	1400	103.3500
07.0000	00	0111	0000	0000	0000	0000	1051	88.49	1400	102.3500
08.0000	00	1000	0000	0000	0000	0000	1151	87.49	1400	101.3500
09.0000	00	1001	0000	0000	0000	0000	1251	86.49	1400	100.3500
10.0000	01	0000	0000	0000	0000	0000	1351	85.49	1400	91.3500
20.0000	10	0000	0000	0000	0000	0000	2351	75.49	1400	89.3500
29.9999	10	1001	1001	1001	1001	1001	3449	64.51	1499	79.3501

4.2 Subassembly Operation

4.2.1 RF Module A6

4.2.1.1 Standard Version (CPN 790-1048-008/-020)

Refer to the appropriate schematic in the diagrams section. The received rf signal enters the 651S-1/1A at rear-panel coaxial connector J61 and is applied directly to low-pass filter FL201. The rf input is then applied to connector P5 on rf module A6 and is routed through low-pass filter FL501 on A6 to 1 of the diode-switched bandpass filters on A6. Functionally, the -008 and -020 part numbers are identical. The -008 has 10 diode-switched bandpass filters and the -020 has only 3 diode-switched bandpass filters. The -020 part number is the current production model.

The proper filter is selected by band information from band decoder card A7 (refer to table 5 for the outputs from card A7). For example, if an operating frequency within the 3- to 3.9999-MHz band is selected, +5 V appears at A6P8-7 and -15 V is applied to all other band inputs. The +5 V at A6P8-7 forward biases diode CR113, allowing the rf input signal to pass through the 3- to 3.9999-MHz bandpass filter. The -15 V on the other band inputs disables the remaining bandpass filters.

The received rf input passes through the selected bandpass filter and is transformer coupled to multiple FET mixer U1 where a variable injection signal from 79.3501 to 109.10 MHz is added to produce a 109.35-MHz signal. (For example, if the operating frequency is 2.901 MHz, the injection signal supplied by the synthesizer is 106.449 MHz.) The injection frequencies are applied through broadband injection amplifier Q5. The injection amplifier uses feedback control to eliminate gain and sensitivity changes due to varying injection voltages across the frequency spectrum. Resonant transformer T2 matches the output of mixer U1 to 109.35-MHz crystal filter FL1. This crystal filter has a 16-kHz bandwidth.

After passing through crystal filter FL1, the 109.35-MHz signal is applied to an FET balanced mixer (Q1 and Q2) where 99 MHz is injected and the 109.35-MHz signal is converted to 10.35 MHz. The injection signal is supplied by the synthesizer cards and is amplified by transistor A6Q6. The mixed signal is applied through resonant transformer T4 to if amplifier A3. AGC is applied at this point and the final 10.35-MHz signal is sent to if filter card A5.

4.2.1.2 VLF Version (CPN 790-1048-010/-021)

Refer to the appropriate schematic in the diagrams section. The received signal is applied to A6P5 and then to K701. If the incoming signal is above 560 kHz, K701 is deenergized and the rf is applied to the filter assemblies and everything is as in the CPN 790-1048-008/-020 versions of A6.

If the incoming signal is below 560 kHz, K701 is energized and the rf is applied to the vlf up-converter (sheet 2 of the schematic). The signal is filtered by FL601 and applied to balanced FET mixer U601 and mixed with 9.9-MHz. The output range of frequencies from this mixer is 9.912 MHz to 10.4599 MHz.

This range of outputs is then applied to multiple FET mixer U1 and the signal is processed as in the CPN 790-1048-008/-020 versions of A6.

4.2.2 IF Filter Card A5

Refer to the schematic in the diagrams section. The if filter card is subcard A5A1 only for standard bandwidths; however, optional filter A5A1FL1 is added and/or subcard A5A2 is sandwiched with A5A1 to provide optional bandwidths. Refer to table 1 and paragraph 5 for receiver configuration/subcard part number information. Also refer to table 1 in the optional section for the operational bandwidths available with respect to the mode switch positions required to enable the proper filter.

The 50-ohm, 10.35-MHz if signal from rf module A6 comes in at A5P5 and is switched through one of three 10.35-MHz crystal filters, or the filters are bypassed. The signal is applied through A5A1FL1 (optional bandwidth) if BANDWIDTH .5, CW, or 2 (as appropriate) is selected, through A5A2FL2 (optional bandwidth) if BANDWIDTH 1, 4, WSRT, or WBTY (as appropriate) is selected, or through A5A2FL3 (optional bandwidth) if BANDWIDTH 3 is selected. For all other modes, these three filters are bypassed and the 10.35-MHz signal is applied through an 8-dB pad (made up of A5A1R2, R3, and R4). When the operating bandwidth is selected, transistor gates switch

the appropriate filter (or the pad) into the signal circuit. This switching differs when certain subcards are used; refer to paragraph 5 for differences. The resultant 10.35-MHz signal is then converted to 450 kHz by balanced FET mixer Q9 and Q10. The 9.9-MHz mixing injection signal is supplied by the synthesizer cards and is controlled by buffer amplifier A11.

The 450-kHz signal is then applied through tuned transformer T2 to another group of filters; either a 450-kHz AM, USB, or LSB mechanical filter; an optional-bandwidth crystal filter A5A2FL4 for BANDWIDTH .2, 1, or NSRT (as appropriate) or an 8-dB pad (A5A1C50, R64, and C51) for 16-kHz bandwidths of AM and FM. If operating in the optional ISB mode, the LSB mechanical filter passes the ISB signal. The inputs and outputs of the mechanical filters are tuned by fixed capacitors. The appropriate filter is again selected by enabling the correct transistor gate. The FET's at the filter outputs serve as low-noise if preamplifiers and the final 450-kHz signal is routed to if amplifier card A4.

4.2.3 IF Amplifier Card A4

Refer to the appropriate schematic in the diagrams section. If amplifier card CPN 778-2951-001 is the standard if amplifier card with FM. The -003 and -004 part numbers are functionally identical to the -001 except the -003 provides for a special fast reaction external rf gain control and the -004 has no FM detector. The -004 part number is the current production model. Refer to table 1 and paragraph 5 for receiver configuration and difference data.

The 50-ohm, 450-kHz if signal from if filter card A5 passes through 1:5 step-up transformer T1 and three transistor amplifiers Q1, Q2, and Q3 on if amplifier card A4. Shunt diode AGC is applied to each of the three transistor amplifiers. The 450-kHz signal then branches four ways: one for if output, one for AM/AGC detection, one for SSB/CW detection, and one for NBFM detection.

The signal for if output passes through two additional transistor amplifiers, Q6 and Q7, to emitter follower Q8. The output from Q8 is routed through 3:1 step-down transformer T2 to output connector P3 on the rear of the chassis.

The signal for SSB/CW detection passes through transistor amplifier Q4 and 1:4 voltage step-up transformer T3 to dual-gate FET product detector Q12. The bfo signal is injected at this point to derive the SSB/CW intelligence. The SSB/CW signal is then routed to audio amplifier card A2.

The signal for AM/AGC detection is applied to AGC amplifier transistors Q10 and Q11. The output from Q11 is transformed and then demodulated by emitter follower Q13. This signal is the AM audio signal and is sent to audio card A2. The signal for FM is taken from the high-level output of AGC amplifier Q10 and is applied to buffer transistor Q12. The FM signal is then applied to FM limiter/detector U2 and the audio output is sent separately to audio card A2.

The output from AGC amplifier transistors Q10 and Q11 is also applied to an adjustable AGC time constant circuit. The AGC release time is controlled at this point by an AGC release time control input from DCFE card A8 or the AGC FAST-SLOW front panel switch. The AGC line is highly filtered to protect against in-band intermodulation. The dc level of AGC is amplified by operational amplifier U1 and complementary emitter follower Q17 then drives the AGC bus. AGC can also be completely disabled by the front panel switch (center position), or by DCFE card A8.

4.2.4 ISB Amplifier Card A3 (Optional)

Refer to the schematic in the diagrams section. In the ISB mode of operation, the signal passing through the LSB mechanical filter on if filter card A5 is applied to ISB if input connector P1 on ISB amplifier card A3. This signal is processed the same as the if signal on if amplifier card A4 (see paragraph 4.4 for circuit operation). ISB if and AM audio signals are developed and appear as outputs from card A3. The SSB af signal developed by dual-gate FET product detector Q12, however, is not sent by card A3 to audio card A2. This signal is routed through operational amplifiers U2A, U2B, and U3 and transformer T5. The output from T5 is a separate 600-ohm ISB audio signal.

4.2.5 Audio Card A2

Refer to the appropriate schematic in the diagrams section.

All audio signals are fed to audio card A2 for final amplification. The three types of signal (AM, FM, and SSB/CW) are applied to gated amplifiers. The appropriate type signal is passed and amplified when the front-panel mode selector is in the proper position to enable the selective gate. The selected audio signal is applied to linear operational amplifiers U3A and U3B through blanking gate transistor Q15. Two types of audio output are developed, 600-ohm line output for external power amplification and 8- to 600-ohm loudspeaker/headset output.

The 600-ohm output is developed through operational amplifier U4 and 600-ohm center-tap transformer T1. The loudspeaker/headset output goes through the front-panel volume control to a power amplifier mounted on the rear chassis.

Fixed bfo signals from synthesizer reference card A11 are routed through card A2 directly to if amplifier card A4. In local control, front panel control switch S105 (BFO switch) selects either a fixed (450 kHz) or variable bfo (vbfo) frequency. When BFO switch S105 is in the FIXED position, logic 0's are applied by interconnect card A8 to interpolate vbfo enable pin A2P1-43 and to CW vbfo enable pin A2P1-41. These logic 0's turn off transistors A2Q3 and A2Q4, disabling crystal oscillators A2Y1 and A2Y2. The fixed 450-kHz bfo input frequency, phase-locked to the 9.9-MHz reference frequency, is then applied to 450-kHz bfo input connector A2P3 by synthesizer reference card A11. The bfo frequency is then diode switched by A2CR7 and A2CR8 to bfo output connector A2P2.

Circuit card A2 also generates the vbfo signals and routes these signals to if amplifier card A4. The vbfo circuits produce bfo variations in SSB of ±60 Hz in 10-Hz steps and in CW of ±900 Hz.

When BFO switch S105 is in the VAR position and USB or LSB mode is selected by front panel mode switch S102, a logic 1 is applied to interpolate vbfo enable pin A2P1-43 by interconnect card A8. This logic 1 turns on transistor A2Q3, enabling crystal oscillators A2Y1 and A2Y2. A 3- to 12-Vdc vbfo signal from 13-position front panel VBFO control switch S112 is applied to vbfo frequency input pin A2P1-45. This variable voltage is divided by resistor networks on card A2 and is applied to Varicaps A2CR1 and A2CR3. These Varicaps then pull the crystal oscillators, resulting in variable frequency outputs from the crystal oscillators. These outputs are applied to and mixed by mixer A2U1 to produce the bfo variation in SSB of ±60 Hz. On audio card A2 (CPN 778-2948-002) and the older versions of -003 (refer to paragraph 5 for difference data), this signal is amplified by operational amplifier A2U2 and routed through low-pass filter circuit (A2T1, -T2, -C42, -C43, and -C44) to BFO output connector A2P2. The low-pass filter shapes the bfo output sine-wave signal and prevents the oscillator frequencies (4.00 and 4.45 MHz) from being applied to the bfo output line. On audio card A2 (CPN 778-2948-004) and the current production model of -003, -005, the bfo variation signal is amplified by transistor amplifier Q6 and routed to bfo output connector A2P2.

When BFO switch S105 is in the VAR position and CW mode is selected by front panel mode switch S102, a logic 1 is applied to CW vbfo enable pin A2P1-41 by interconnect card A8. This logic 1 turns on transistor A2Q3, enabling crystal oscillators A2Y1 and A2Y2 and turns on transistor A2Q4, energizing relays A2K1 and A2K2. The 13-step vbfo control signal from front panel switch S112 is applied to vbfo frequency input pin A2P1-45 as in USB or LSB mode. However, in CW mode, relays A2K1 and A2K2 switch different resistors into the divider circuits and different fixed capacitors into the oscillator circuits. The crystal oscillators then produce different frequencies when pulled by Varicaps A2CR1 and A2CR3. The outputs from the oscillators are applied to and mixed by mixer A2U1 as in SSB. The output from the mixer in CW mode, however, is a bfo variation of ±900 Hz. The signal is then amplified and routed to bfo output connector A2P2 as in SSB.

In remote control, the operation of the bfo and vbfo circuits on audio card A2 is the same as in local control. The interpolated vbfo enable, CW vbfo enable, and vbfo frequency control inputs to card A2, however, are generated by control word commands from the associated processor unit. Refer to the DCFE theory of operation for control word content and format.

The optional squelch circuit on audio card A2 (CPN 778-2948-002/-004) consists of two integrated active filters (high pass U1A and low pass U1B), two rectifier transistors Q1 and Q2, and differential amplifier U2 that compares the rectified levels from Q1 and Q2.

The output from U2 controls gating transistors that turn on squelch gate Q15. Squelch gate Q15 is also controlled by squelch on/off and audio blanking signals. The squelch on/off control signal is sent from the front panel SQUELCH control or DCFE card A8. The audio blanking signal is developed when manual tuning is initiated and blanks out the audio signal until a new operating frequency is selected by the manual tuning control.

The squelch level input is developed by the front panel SQUELCH control. Received speech signals have a greater level of low-frequency components than high-frequency components. The squelch level signals are therefore applied to the output of low-pass filter U1B.

4.2.6 Synthesizer Divider Card A10

4.2.6.1 Standard Version (CPN 793-9334-002)

Refer to the schematic in the diagrams section. The circuits on synthesizer divider card A10 form a programmable frequency divider with variable division ratios ranging from 391 through 3449. The division ratio for a particular operating frequency is determined by the bcd frequency control information from card A8 or card A14 plus fixed number 351. The variable divider contains two programmable decade counters and one programmable digit counter. The first decade counter consists of U21, U11, U13, U14, U24, and U34; the second decade counter consists of U41, U23, U54, U22, and U73; and the digit counter consists of U71, U61, and U72.

A 3- through 35-MHz input is applied to the first programmable decade counter. Frequency control information is applied to converter circuits within the variable counter circuits in parallel binary bcd form. The 10-kHz output is applied to the phase-locked loop phase detector on synthesizer reference card A11.

Altering the count of the first decade counter by 1 during each count cycle will change the net division ratio of the complete circuit by 1. Therefore the first decade is controlled by the 100-Hz and 10-kHz frequency control information in addition to a fixed number 1 (the 1 of the fixed number 351). Similarly, altering the count of the second decade by 1 during each count cycle changes the net division ratio of the complete circuit by 10. The second decade then is controlled by the 1-kHz and 100-kHz frequency control information in addition to a fixed number 5 (the 5 of the fixed number 351). Altering the count of the programmable digit counter by 1 during each count changes the overall net division ratio by 100. This section then is controlled by the 1-MHz and 10-MHz frequency control information along with the fixed number 3 (the 3 of the fixed number 351). The net division ratio of the complete variable divider circuit can be determined as shown in the following example.

	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz
Operating frequency	0	2	0	0	9	9
Add 1-kHz and 100-Hz digits			9	9		
Add fixed number	0	3	5	1		
Total	0	6	5	0		

Determine the division ratio by adding 6, 5, and 0 as follows:

6 = 600

5 = 50

0 = 0

Division ratio = 650

The following explanation describes the general events that occur in the 10-kHz phase-lock loop when the operating frequency is changed in small steps.

Assume that the phase-lock loop is in an in-lock condition, which means that both inputs to the phase detector circuits are 10 kHz. When the operating frequency of the radio set is changed, the division ratio of the programmable divider circuits also changes and causes the output of the divider circuits to be some value other than 10 kHz. The output pulse width of the phase detector circuit on card A11 changes and applies a different error voltage level to the vco on card A13. When the error voltage is applied, the vco begins to change frequency and continues to change until the output of the divider circuit is again 10 kHz. At this point the output pulse width of the phase detector stops changing, the vco remains at that frequency, and the 10-kHz phase-lock loop is again in an in-lock condition. The phase detector controls both frequency and phase. For small frequency changes as just described, the frequency function of the detector does not operate, but for large frequency changes, the phase function is inhibited and the output of the detector locks in a high or low state. It remains in this state until the vco frequency passes through the desired value, at which time it switches back to the phase detection mode.

4.2.6.2 VLF Version (CPN 793-9334-006)

At 560 kHz and above, the vlf version of A10 functions the same as card A10 (CPN 793-9334-002). However, below 560 kHz, combinational logic circuits alter the 10-MHz, 1-MHz, and 100-kHz inputs by adding 9.9 MHz to the incoming signals. For example, if 12 kHz is the incoming control frequency, the synthesizer is directed to act as if 9.912 MHz was received. The resulting synthesizer injection frequencies are actually 9.9 MHz above the vlf selected frequencies.

4.2.7 Synthesizer Reference Card A11

Refer to the schematic in the diagrams section. Synthesizer reference card A11 provides all reference signals required by the synthesizer circuits as well as the injection signals to the if/af cards, and rf module. It contains the 9.9-MHz frequency standard, multiplier, fixed dividers, and phase detectors for both phase-locked loops 1 and 2.

Frequency standard A1 is a temperature-compensated 9.9-MHz crystal-controlled oscillator. Buffer/driver circuit U45 is used primarily for signal distribution. It also prevents loading of the frequency standard and isolates the digital circuits from the 9.9-MHz output and X10 multiplier A2.

The X10 multiplier multiplies the 9.9-MHz reference frequency by 10 to provide two fixed 99-MHz injection frequencies for use in the phase-locked loop 2 mixer (on synthesizer mixer card A12) and the rf mixers on rf module A6.

The 9.9-MHz filter (L5, C17, and C18) provides impedance matching and harmonic filtering for the 9.9-MHz injection frequency applied to if filter card A5. The 9.9-MHz frequency standard is fed through three fixed divide-by-10 decade counters (U25, U13, and U12) to provide the 9.9-kHz reference frequency to loop 1 phase detector circuit U21, U31, U41, and U42.

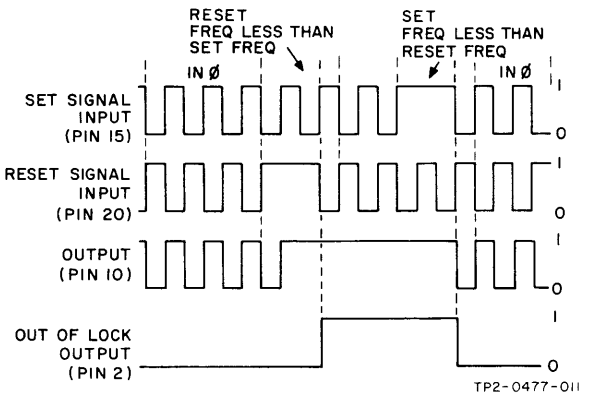
The output of divide-by-10 decade counter U25 is also applied to a divide-by-99 counter circuit to provide the 10.0-kHz reference frequency to loop 2 phase detector circuit U34, U44, U43, and U33. The divide-by-99 counter is formed by two 4-binary counters (U23 and U24) plus two logic gates U11A and U11B). U23 is connected as a divide-by-nine decade counter and the output of U23 (110 kHz) is applied to the divide-by-11 decade counter (U24). The 10-kHz output of U24 is applied to the phase detector circuit. Logic gates U11A and U11B improve the waveshape of the output pulse.

The 9.9-MHz frequency standard is also applied to a divide-by-two counter (U14B). The 4.95-MHz output of this circuit is applied to a divide-by-11 decade counter U15 to provide the 450-kHz injection signal for the if/af cards. L1 and C3 through C5 form a pi-section LC filter to provide impedance matching and harmonic filtering for the 450-kHz injection signal.

The phase detector circuits for phase-locked loops 1 and 2 are identical. They provide positive output pulses at their respective frequencies (9.9 kHz/10 kHz) to the low-pass filter drivers on synthesizer vco card A13. Since both detectors are functionally the same, only the operation of loop 1 detector circuit will be discussed.

Phase detector U21 receives two input signals: a 9.9-kHz reference or set signal (U21B), and a 9.9-kHz reset signal from phase-locked loop 1 variable dividers (U21A). The detector circuit compares the phase relationship of the set and reset input signals and generates an output pulse, the width of which is equal to the phase difference between two inputs (figure 6). If the reset input falls below 9.9 kHz, the resulting phase differential causes the error output to lock at logic 1. If the reset signal rises above 9.9 kHz, the error output locks at logic 0. The output remains at logic 1 or logic 0 until the vco passes through the desired in-lock frequency. It then starts responding again to the set and reset inputs. The phase detector circuit is totally unaffected by harmonics of the basic frequencies involved in the phase-lock loop. The error output of the detector is applied to low-pass filter driver Q3 on synthesizer vco card A13.

Out-of-lock monitor U32 output is a logic 0 when either loop 1 or loop 2 is in an in-lock condition. When either loop is in an out-of-lock condition, out-of-lock monitor output goes to logic 1 indicating to monitor circuits on DCFE card A8 that one of the phase-lock loops is not operating properly.



Frequency Phase Detector Timing Diagram
Figure 6

4.2.8 Synthesizer Mixer Card A12

Refer to the schematic in the diagrams section. Synthesizer mixer card A12 is comprised of phase-locked loops 1 and 2 mixers and the variable divider circuit used in loop 1.

The 79.3501- to 109.100-MHz signal from loop 1 vco is applied to loop 1 mixer A1 along with the 64.510- to 95.240-MHz signal from loop 2 vco. The difference frequency from A1 ranges from 13.860 to 14.840 MHz and is applied through inverter amplifier U11B to the variable frequency divider circuit.

The variable divider circuit used in loop 1 is a programmable frequency divider with variable division ratios ranging from 1400 through 1499. The division ratio for a particular operating frequency of the radio set is determined by the 100-Hz and 1-kHz frequency information from frequency control card A14 or DCFE card A8. The divide-by-100-to-199 circuit consists of two decade programmable counters: U1 through U5 and U7 form the first decade counter, and U9 the second.

The bcd frequency control information (100 Hz and 1 kHz) is applied to code converter circuits within the counter circuits that inhibit the decade counters for a number of pulses equal to the 100-Hz and 1-kHz value (digit) of the operating frequency. If the 100-Hz and 1-kHz digits are both 0, the counters are not inhibited and function as basic decade (divide by 10) counters. If the digits are both 9, the counters are both inhibited for 9 pulses prior to dividing by 10.

In the first instance, the resulting count (division ratio) is 100. In the second instance, the division ratio is 199.

The remaining counter circuit U10 is a fixed divide-by-14 binary counter circuit that, when operating in series with division ratios ranging from 100 to 199, provides an overall division ratio of 1400 to 1499. Table 5 provides the division ratios of the 9.9-kHz divider circuits for various operating frequencies. The division ratio for any operating frequency can be calculated as follows:

Operating frequency: 2.0049 MHz

Fixed division ratio:	1	4	0	0
Add 1-kHz digit:			4	
Add 100-Hz digit:				9
Total (division ratio):	1	4	4	9

The 9.9-kHz output signal is applied to the phase detector on synthesizer reference card A11.

The 64.510- to 95.24-MHz signal from loop 2 vco is applied to loop 2 mixer A2 along with the 99-MHz injection frequency from the X10 multiplier on synthesizer reference card A11. The difference frequency of A2 ranges from 3.76 to 34.490 MHz and is applied to the input of phase-locked loop 2 variable divider circuit on synthesizer divider card A10.

4.2.9 Synthesizer VCO Card A13

Refer to the schematic in the diagrams section. Synthesizer vco card A13 receives phase detector outputs from synthesizer reference card A11 and provides injection outputs to synthesizer mixer card A12 and rf module A6.

The 10-kHz input at P1 is positive pulses from the phase detector on synthesizer reference card A11. The width of the positive pulses is proportional to the phase error. When the phase error increases, the width of the positive pulses also increases. The positive pulses are amplified by driver Q2 and applied to the loop 2 low-pass filter. The low-pass filter provides a positive dc output to the vco (voltage controlled oscillator) that is proportional to the width of the square-wave input.

The loop 2 vco generates two identical 64.510- to 95.24-MHz output frequencies that are supplied to synthesizer mixer card A12. The loop 2 vco also provides positive and negative voltage outputs to the loop 1 vco. The vco contains an FET oscillator that is controlled by a varactor with the varactor controlled by the positive voltage output of the low-pass filter. As the positive voltage output of the low-pass filter increases, the frequency output of the vco increases.

The loop 1 low-pass filter and vco operate similarly to the loop 2 low-pass filter and vco. The loop 1 vco is controlled by outputs from the loop 1 low-pass filter and the loop 2 vco. The loop 1 vco supplies two identical 79.3501- to 109.100-MHz outputs, one to rf module A6 and the other to synthesizer mixer card A12.

4.2.10 Decoder/Driver Card A7

Table 5 lists the logic inputs to card A7 and A7's outputs to module A6.

4.2.10.1 Decoder/Driver A7, 778-2928-003

Refer to the schematic in the diagrams section. The decoder/driver card converts the bcd frequency information from frequency control card A14 into 10 frequency band outputs. The individual circuits that produce the 10 bands are similar; only the 16- to 23.9999-MHz enabling circuit and how the other bands are disabled are described. For this purpose, assume an input frequency of 18 MHz.

The 10-MHz-2 and 1-MHz-4, -2 and -1 input lines are logic 0, and the 10-MHz-1 and 1-MHz-8 input lines are logic 1.

The 10-MHz-2 (logic 0) input is inverted by U1D and U1E with the U1E logic 0 output applied to U6A-3 as an enabling signal and to U11C-8 and U11D-12 as a disabling signal. The U1E output is also inverted by U1F to logic 1 and applied to U6B-6 as a disabling signal and to U15B-5.

The 10 MHz-1 (logic 1) input is inverted by U1A and U1B with the U1B logic 1 output applied to U7C-11 and U11B-6 as an enabling signal and

Table 5. Decoder/Driver Input/Output Table.

		OPERATING BAND (MHz)																																					
		29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	.9	.8	.7	.6	.56	.5	.4
Bcd input to A7	20	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	2	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
	0.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
	0.08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0.04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0.02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Band output to A6	24-29.9999	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16-23.9999	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	12-15.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8-11.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6-7.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	4-5.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	3-3.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	2-2.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	0.56-1.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
	0-0.5599	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

CPN 608-9087-001 and 608-9121-001 each has only 3-band output: Band 1, 0 to 0.5599 MHz; band 2, 0.56 to 1.9999 MHz, and band 3, 2 to 29.9999 MHz.

to U8A-3, U8C-11, and U8B-6 as a disabling signal. The U1B output is also inverted by U1C to logic 0 and applied to U6B-8 as a disabling signal and to U15B-6. The U15B logic 1 output is inverted by U16A and this logic 0 is applied as a disabling input to U7A-2, U7B-6, and U14B-5.

The 1 MHz-8 (logic 1) input is inverted by U3D and U3E with the U3E logic 1 output applied to U11B-5 as an enabling signal and to U11C-9 and U14B-6 as a disabling signal. The U3E output is also inverted by U3F to logic 0 and applied to U6A-1 as an enabling signal and to U15A-1.

The 1 MHz-4 (logic 0) input is inverted by U3A and U3B with the U3B logic 0 output applied to U7C-13 as an enabling signal and to U8C-13, U7A-3, U7B-7, and U11D-13 as a disabling signal. The U3B output is also inverted by U3C to logic 1 and applied to U6A-2 as an enabling signal and to U8A-1, U8B-7, and U6B-7 as a disabling signal.

The 1 MHz-2 (logic 0) input is inverted by U2A and U2B with the U2B logic 0 output applied to U7C-12 as an enabling signal and to U7A-1, U8A-2, U12A-1, and U12C-12 as a disabling signal. The U2B output is also inverted by U2C to logic 1 and applied to U7B-8 as a disabling signal and to U15A-2. The U15A logic 1 output is inverted by U16B to logic 0 and applied to U8B-8, U8C-12, and U13A-1 as a disabling input.

The 1 MHz-1 (logic 0) input is inverted by U2D and U2E with the U2E logic 0 output applied to U12A-2 as a disabling signal. The U2E output is also inverted by U2F to logic 1 and applied to U12C-13 and U13C-9 as a disabling signal.

The 18-MHz enabling decode circuit consists of U6A, U7C, and U11B. The enabling signals derived above for this circuit are two logic 0's and one logic 1 for the U6A and U7C, and two logic 1's for U11B. The two logic 1's and one logic 0 output of this circuit are applied to U6C. The U6C logic 1 output turns on Q3 and in turn Q4 turns on. This produces a logic 1 (+5 Vdc) output at P1-45 (16- to 23.9999-MHz enable).

The disabling logic (for all frequencies except 18 MHz) derived above acts to cut off the output band-driver circuits. The 24- to 29.9999-MHz band is disabled by disabling logic on U11C and U11D. A logic 1 and a logic 0 input to U11C and two logic 0 inputs to U11D produce two logic 1 outputs. Two logic 1 inputs to U11A produce a logic 0 output. This cuts off Q1 and Q2 in turn. Pin P1-62 (24 to 29.9999 MHz) then has a logic 0 (-15 Vdc) as an output to the band circuits of rf module A6. The 12- to 15.9999-MHz and the 8- to 11.9999-MHz bands are similarly disabled.

The 6- to 7.9999-MHz band is disabled by U7A. The disabling logic (all 0's for U7A) produces a logic 1 at U7A-5. This prevents VR1 from breaking down and keeps Q9 cut off. Pin P1-43 then has a logic 0 (-15 Vdc) as an output to the band circuits of rf module A6. The 4- to 5.9999-MHz, the 3- to 3.9999-MHz, the 2- to 2.9999-MHz, the 560-kHz to 1.9999-MHz, and the 0 to 560-kHz bands are similarly disabled.

4.2.10.2 Decoder/Driver Card A7 608-9087-001

Refer to the schematic in the diagrams section. The decoder/driver card converts the bcd frequency information from frequency control card A14 into three frequency band outputs: band 1, 0 to 0.5599 MHz; band 2, 0.5600 to 1.9999 MHz; and band 3, 2 to 29.9999 MHz. The operation of each band is described using one assumed input frequency in each band.

On band 1, assume an input frequency of 440 kHz. The 10-MHz and 1-MHz input lines are logic 0; the 100-kHz-2-8 and 10-kHz-8-2 input lines are logic 0, and the 100-kHz-4 and 10-kHz-4 input lines are logic 1.

The logic 0 on the 10-MHz and 1-MHz input lines to the base of Q1 maintains Q1 in an off state. The +5 Vdc (logic 1) on the collector of Q1 cuts off Q2 and disables band 3 (pin P1-56). The logic 1 from the collector of Q1 is applied as one of the enabling signals to the input of U3A.

The other enabling signals for U3A (band 1) are derived from the logic inputs to the 10-kHz, 100-kHz, and 1-MHz-1 input lines. The 10-kHz-2 (logic 0) and -4 (logic 1) are applied to U1B. The logic 1 output of U1B is applied to U1C, the 10-kHz-8 (logic 0) is inverted by U2C and applied to U1C. The logic 0 output of U1C is applied to U3B-9 and 10. The 100-kHz-1 (logic 0) and -4 (logic 1) are applied to U3B. The logic 1 output of U3B is applied to U3A-5. The 100-kHz-2 (logic 0) and -4 (logic 1) are applied to U1A. The

logic 1 output of U1A is applied to U1D, the 100-kHz-8 (logic 0) is inverted by U2B and applied to U1D. The logic 0 output of U1D is inverted by U2E and applied to U3A-4. The 1-MHz-1 (logic 0) is inverted by U2F and applied to U3A-2. The logic 0 output of U3A enables Q3 and in turn enables band 1 (pin P1-86). The logic 0 output of U3A is applied through CR7 as a disabling signal to band 2 (U2D and Q4).

To enable band 2, assume an input frequency of 1 MHz. All bcd input lines are at logic 0 except 1 MHz-1. The 1-MHz-1 (logic 1) is inverted by U2F and applied to U3A-2, the output of U3A goes to a logic 1 that disables Q3 (band 1) and is inverted by U2D and applied to Q4. Q4 conducts, and band 2 (pin P1-84) is enabled.

To enable band 3, assume any input frequency between 2 and 29.9999 MHz. A logic 1 on the 10-MHz input lines or the 1-MHz-2, -4, -8 input lines will cause Q1 to conduct; the logic 0 output of Q1 turns on Q2 and enables band 3 (pin P1-56). Simultaneously the logic 0 output of Q1 disables U3A (band 1) and is applied through CR6 and U2D as a disabling signal to Q4 (band 2).

4.2.10.3 Decoder/Driver Card A7 608-9621-001

Refer to the schematic in the diagrams section. Decoder/driver card 608-9121-001 is functionally the same as decoder/driver card 608-9087-001 except in addition to the 3-band output, all bcd inputs are routed through two buffer stages (inverters) and applied to P1 as bcd outputs. Bcd information is required when an external preselector is used with the 651S-1/1A.

4.2.11 Frequency Control Card A14

Refer to the schematic in the diagrams section. Frequency control card A14 receives frequency control inputs from the following three front-panel tuning controls: 1-MHz control S111 that selects frequencies in 1-MHz steps, 0.1-MHz control S110 that selects frequencies in 0.1-MHz steps, and variable tuning control S109 that selects frequencies in 100-Hz steps.

Card A14 converts the frequency information from the front-panel controls to 22-bit bcd parallel data. This frequency data is sent to the frequency synthesizer cards and to the bcd to 7-bar decoder/driver circuits on card A14. The 7-bar decoder/drivers control the 7-bar numeric readout tubes on the front panel of the receiver (refer to the chassis schematic in the diagrams section).

Card A14 uses 5 up-down bcd counters to develop 20 bits of the 22-bit bcd frequency information. These counter outputs represent 100-Hz, 1-kHz, 10-kHz, 0.1-MHz, and 1-MHz 4-bit bcd (1, 2, 4, and 8) frequency information. The remaining 2 bits, representing 10-MHz, 2-bit bcd (1 and 2) frequency information, are developed by flip-flops U27 and U34 on card A14. Each up-down counter controls a 7-bar decoder/driver, and flip-flops U27 and U34 control a 7-bar decoder/driver.

4.2.11.1 Counter Operation

Up-down counters U21 through U25 require certain inputs for proper operation. A logic 1 signal must be applied to count enable input pins 13 through 18 and to parallel entry enable pin 23. A count direction signal (logic 1 for up, logic 0 for down) must be applied to pin 2, and a clock pulse must be applied to pin 1.

The logic 1 parallel entry enable signal on pin 23 is provided by Q7. This logic 1 also enables the first stage of NAND gates following each up-down counter, allowing the outputs from each counter to be inverted by these NAND gates.

The logic 1 count enable signals on pins 13 through 18 are provided by a +5-Vdc keep-alive voltage and by terminal count signals from preceding up-down counters. A terminal count logic 1 output appears at pin 11 of an up-down counter when the counter reaches state 9 (1001) and the count direction signal is logic 1 (up), or when the counter reaches state 0 (0000) and the count direction signal is logic 0 (down).

The local/remote line is logic 1 during local operation. This logic 1 enables the second stage of NAND gates following each up-down counter, allowing a second inversion of the up-down counter outputs. The outputs from these NAND gates are routed to the frequency synthesizer cards and to the bcd to 7-bar decoder/drivers on card A14. The local/remote line is logic 0 during remote operation. This logic 0 disables the second stage of NAND gates, allowing remote frequency information to be fed into the control card.

The clock pulse and count direction signals are generated when any one of the three front-panel frequency controls is changed. Three clock pulse signals (CP, CP', and CP") and three up-down signals (U/D, U/D', and U/D") are developed by card A14.

Clock pulse CP is developed when the position of variable tuning control S109 on the front panel is changed. This clock pulse is applied to terminal 1 of up-down counters U21, U22, and U23, and to gate U32B. Clock pulse CP1 is developed either by clock pulse CP or by changing the position of 0.1-MHz control S110 on the front panel. This clock pulse is gated through U32B, inverted by U31D, and applied to terminal 1 of up-down counter U24 and gate U40B. Clock pulse CP" is developed either by clock pulse CP' (which can be developed by clock pulse CP) or by changing the position of 1-MHz control S111 on the front panel. Clock pulse CP" is gated through U40B, inverted by U39D, and is applied to terminal 1 of up-down counter U25 and to the clock inputs of flip-flops U27 and U34.

The three clock pulses permit tuning in 100-Hz, 0.1-MHz, or 1-MHz steps. A clock pulse, however, does not produce a count change from an up-down counter output unless a terminal count signal (logic 1) has been received from the preceding up-down counter (or counters). For example, if tuning were progressing upward in 100-Hz steps, a 1-kHz count pulse from counter U22 would be developed only on the pulse following the 900-Hz count pulse from counter U21.

On 0.1-MHz counter Q24 and 1-MHz counter U25, a terminal count signal may be forced by one of the front-panel frequency controls. As the 0.1-MHz control S110 is being rotated through position A or B, a logic 0 is applied to input pin 13 of gate U30C. This logic 0 forces a logic 1 input to count enable pins 13, 14, and 15 of up-down counter U24 and permits tuning in 0.1-MHz steps. Likewise, as the 1-MHz control S111 is being rotated through position A or B, a logic 1 is applied to pins 13, 14, and 15 on counter U25 and permits tuning in 1-MHz steps. When either switch S110 or S111 is turned one position clockwise, contacts A and B are shorted, then opened in the detent position. Contact C is shorted in the detent position.

The up-down signals are developed by the same controls that produce the clock pulse signals. Signal U/D is developed by changing the position of variable tuning control S109 on the front panel, signal U/D' is developed either by signal U/D or by changing the position of 0.1-MHz control S110 on the front panel, and signal U/D" is developed by signal U/D' or by changing the position of 1-MHz control S111 on the front panel. The up-down signals indicate the direction of change of the up-down counters. A logic 1 up-down signal produces a count increase with a properly enabled clock pulse and a logic 0 produces a count decrease with a properly enabled clock pulse.

4.2.11.2 Local/Remote Control

Local or remote control is selected by LOCAL/REMOTE switch S108 on the front panel. In local operation, a logic 1 input is applied to pin P1-57 on card A14 by LOCAL/REMOTE switch S108. This logic 1 is inverted by U36B and the resulting logic 0 disables remote frequency load gate U35D. The logic 1 at P1-57 is also applied to gates U36A, U37A, U37B, U29C, and to the second stage of NAND gates following each up-down counter. The logic 1 on gates U37A and U37B allows the parallel entry enable logic 1 from Q7 to be applied to pin 23 on each up-down counter and to the gates in the first stage of NAND gates following each counter. Normal tuning then proceeds by making use of the three front-panel frequency controls.

DIAL LOCK switch S113 on the front panel is used to prevent accidental change of frequency during local operation. In the LOCK position, switch S113 applies a logic 0 to P1-5 on card A14. This logic 0 disables 100-Hz tuning gate U36A and prevents the recognition of any change in position of variable tuning control S109.

In remote control operation, a logic 0 input is applied to pin P1-57 by LOCAL/REMOTE switch S108. This logic 0 disables gate U36A and prevents and frequency change by the .1 MHZ selector. The logic 0 is also applied to gates U37A, U37B, U29C, and to the second stage of NAND gates following each up-down counter. The resulting logic 1 from U37A turns on transistor Q7 and Q7 turns off all the up-down counters by applying a logic 0 to terminal 23 of each

counter. This logic 0 allows each up-down counter to be preset to the logic levels appearing on pins 19, 20, 21, and 22 in the event of a clock pulse on pin 1. The logic 0 from Q7 also forces a logic 1 output from each gate in the first stage of NAND gates following the up-down counters. The gates in the second stage of NAND gates have logic 0 on the local/remote inputs, resulting in logic states at the outputs from these NAND gates corresponding to the remote bcd frequency data from the DCFE circuits. The frequency load input at A14 P1-64 generates a clock pulse that loads each counter with the logic state appearing at the outputs of the second stage NAND gates.

In remote operation, the inputs to the 7-bar decoder/drivers come from the DCFE circuits, rather than from the second stage of NAND gates following the up-down counters. The bcd frequency information from the DCFE circuits appears on the signal lines that served as outputs to the frequency synthesizer cards during local operation. The bcd to 7-bar decoder/drivers then control the 7-bar numeric readout tubes on the front panel as in local operation.

4.2.12 Power Supply Circuits and Regulator Card A1

Refer to the chassis schematic and card A1 schematic in the diagrams section. The power supply circuits are in two locations in the receiver. The supply circuits are on the rear chassis and the regulator circuits are on card A1. In the chassis circuits, multiple-secondary transformer T201 converts the 115/230 V, 47- to 420-Hz input power to 10-, 15-, and 18-V ac levels. Bridge rectifiers, RC ripple filters, and series regulator transistors provide +5, +25, and -15 Vdc for the regulator card.

Also on the rear chassis are connection points for a 6-V battery (available option). This battery power is used for the +5-VKA (keep-alive voltage) input to frequency control card A14 for up to 30 seconds if a primary power shortage occurs. This prevents A14 from losing frequency information. The battery is switched off when the POWER switch is set to OFF. A lamp on the front will light if primary power is lost and the battery is being drained.

Regulator card A1 uses +25 Vdc to provide +25-Vdc switched, +15-Vdc switched, and +15-Vdc continuous outputs. The +5-Vdc input is used to provide +5 Vdc switched and continuous outputs and the -15-Vdc input is used to provide -15 Vdc switched and continuous outputs.

Integrated circuit regulators are used for all three major inputs. Series regulating transistor Q1 is used in addition to integrated circuit U3 for +5-Vdc regulation.

The +15-Vdc switched, -15-Vdc switched, and +5-Vdc switched outputs are applied to performance monitor gate U4A. This gate activates the fault monitor circuits in the optional DCFE card when optional 3-pair serial digital remote control is employed.

The blanking circuits are also on card A1. An 8-ms blanking pulse is generated on frequency control card A14 any time one of the frequency tuning controls is changed to allow the frequency synthesizer circuits to lock on the newly selected frequency. The circuits on card A1 switch the pulse and apply an af blank signal to audio card A2. The af signals are blanked (muted) to keep background noises out while tuning.

4.2.13 Interconnect Card A8

Refer to the schematic in the diagrams section. Interconnect card A8 routes the manual mode control information and other miscellaneous controlling functions to the various cards and circuits that would be controlled by the optional cards when remote control is employed. Interconnect card A8 is replaced by DCFE card A8 when 3-pair serial digital or teletypewriter code remote control is used (card A9 must also be installed for remote control operation).

4.2.14 DCFE Card A8 (Optional)

Refer to the schematic in the diagrams section. The DCFE (device control functional element) controls all the operations of the receiver based on the commands from the external control. Serial digital control information from the control is demodulated in and gated through DCU card A9, and is applied to the DCFE in serial form. TTY-coded control information is decoded in and gated through TCU card A9, and is applied to the DCFE in serial form. The

DCFE then converts the serial control commands to parallel form and enables or disables the appropriate functions in the receiver.

The control commands to the DCFE are divided into four control words (I, II, III, and IV), and may be sent in any order depending on the processor programming. Word I is frequency control, word II is mode I control, word III is mode II control, and word IV is monitor request. Each word comes in separately, and immediately after the reception of each properly addressed control word, a monitor word is returned to indicate the receiver's reaction to the control word. If the receiver reacted improperly, the control word is retransmitted; if it reacted properly, the next control word will be transmitted. Word IV (monitor request) is repeated continuously until something faults or is changed, to indicate the operational status of the receiver at all times. Table 6 lists the content and format of all the control words. Table 7 shows control word II programming for mode selection.

Other cards in the receiver generate the monitor signals that indicate the operational status of the receiver during the word period immediately following a properly addressed control word. These parallel binary signals are applied to the DCFE for transfer to the processor control unit (through DCU card A9 that converts the parallel data to serial data) or to the TTY (through TCU card A9). The monitor data sampled and sent to the DCFE depends upon the type of control word received. Table 8 lists the content and format of the monitor words.

Table 6. Control Words, Content and Format.

BIT POSITION	CONTROL WORD I (Freq info)	CONTROL WORD II (Mode I info)	CONTROL WORD III (Mode II info)	CONTROL WORD IV (Monitor request)
0	Dialogic bit	Dialogic bit	Dialogic bit	Dialogic bit
1	X	X	X	X
2	X	X	X	X
3	X — 5-bit DCU address	X — 5-bit DCU address	X — 5-bit DCU address	X — 5-bit DCU address
4	X	X	X	X
5	X	X	X	X
6	0 — DCFE subaddress	0 — DCFE subaddress	1 — DCFE subaddress	1 — DCFE subaddress
7	0	1	0	1
8	Parity	Parity	Parity	Parity
9	X	X	X	X
10	(2) — 10 MHz	FM enable	X	X
11	(1)	AM enable	X	X
12	(8) — 1 MHz	SSB/CW enable	X	X
13	(4)	ISB enable	X	X
14	(2)	Fixed BFO enable	X	X
15	(1)	VBFO enable	X	X
16	(8) — 100 kHz	Interpolate enable	X	X
17	(4)	X	X	X
18	(2)	AGC fast enable	X	X
19	(1)	0.2-kHz filter enable — 450-kHz filters	X	X
20	(8) — 10 kHz	2.7-kHz USB filter enable — 450-kHz filters	X	X
21	(4)	2.7-kHz LSB filter enable — 450-kHz filters	X	X
22	(2)	6-kHz filter enable — 450-kHz filters	X	X
23	(1)	450-kHz bypass — 450-kHz filters	X	X
24	(8) — 1 kHz	0.5-kHz filter enable — 10.35-MHz filters	(8) — VBFO	X
25	(4)	1-kHz filter enable — 10.35-MHz filters	(4) — VBFO	X
26	(2)	3-kHz filter enable — 10.35-MHz filters	(2) — VBFO	X
27	(1)	10.35-MHz bypass — 10.35-MHz filters	(1) — VBFO	X
28	(8) — 100 Hz	AGC off	(8) — Rf gain	X
29	(4)	Operate	(4) — Rf gain	X
30	(2)	Local/remote	(2) — Rf gain	X
31	(1)	X	(1) — Rf gain	X

Note: X = don't care

Table 7. Control Word II Mode Selection Programming.

DESIRED MODE OF OPERATION AND BANDWIDTH	WORD II BIT POSITION (LOGIC 1 FOR DESIRED FUNCTION)			
	MODE SELECT	BFO ENABLE (Choose one Only)		
		BFO (Fixed)	VBFO	INTERPOLATE BFO
FM 6 FM 16	10, 22, 27 10, 23, 27, 28			
AM 3 AM 6 AM 16	11, 22, 26 11, 22, 27 11, 23, 27			
SSB 2.7 kHz USB SSB 2.7 kHz LSB ISB	12, 20, 27 12, 21, 27 12, 13, 20, 27	14 14 14		16 16 16
CW .2/1/NSRT CW .5/CW/2 CW 1/4/WSRT/WBTY	12, 19, 24 12, 22, 24 12, 22, 25	14 14 14	15 15 15	

Table 8. Monitor Words, Content and Format.

BIT POSITION	MONITOR WORDS I, III, AND IV	MONITOR WORD II
0	Dialogic bit	Dialogic bit
1	0	0
2	1	1
3	0 *5-bit DCU address	0 *5-bit DCU address
4	1	1
5	0	0
6	0, 1, 1 DCFE subaddress	0 DCFE subaddress
7	0, 0, 1	1
8	Parity	Parity
9	Power interrupt	Power interrupt
10	(2)	Power supply performance
11	(1) 10 MHz	Synthesizer lock
12	(8)	Local/remote
13	(4)	Operate
14	(2) 1 MHz	Audio performance
15	(1)	Store frequency
16	(8)	Mode
17	(4)	Mode
18	(2) 100 kHz	Mode Refer to table 9.
19	(1)	Mode
20	(8)	(8)
21	(4)	(4)
22	(2) 10 kHz	(2) VBFO
23	(1)	(1)
24	(8)	(8)
25	(4)	(4)
26	(2) 1 kHz	(2) 1 kHz
27	(1)	(1)
28	(8)	(8)
29	(4)	(4)
30	(2) 100 Hz	(2) 100 Hz
31	(1)	(1)
*Example address		

Table 9. Mode Selection for Monitor Word II.

MODE	BIT			
	16	17	18	19
FM	0	0	0	0
AM	1	0	0	0
USB, VBFO	0	1	1	0
USB, FIXED BFO	1	1	1	0
LSB, VBFO	0	1	0	1
LSB, FIXED BFO	1	1	0	1
CW, VBFO	0	1	0	0
CW, FIXED BFO	1	1	0	0
ISB, VBFO	0	1	1	1
ISB, FIXED BFO	1	1	1	1

4.2.14.1 Control Word Processing

The control data from the DCU or TCU is applied to the DCFE along with the control gate, monitor gate, bit clock, and weight 4 signals. The control data input to the DCFE consists of bits 6 through 31 of the control word received by the DCU. Bits 0 through 5, dialogic bit, and address bits, are extracted by the DCU or TCU. Bits 6 and 7 (subaddress) of control word define which of the control words (I, II, III, or IV) is present, and bits 8 through 31 contain the control information to be processed by the DCFE for use throughout the receiver. The logic levels of the control gate, monitor gate, monitor data, bit clock, and weight 4 signals are shown in figure 12 (DCU theory).

One of the initial functions of the DCFE is the generation of word I, word II, and word III load commands to enable the loading of the control information (bits 8 through 31) into the proper storage registers. The word I storage registers are U16, U20, U24, U28, U32 and U36; word II storage registers are U19, U23, U27, U31 and U35; and word III storage registers are U34 and U38. Shift register U6 stores the subaddress information from bits 6 and 7 of the control word and provides inputs to the word load gate circuits where the appropriate load gate is generated.

U6 is a 4-bit shift register that provides one of two alternate shift modes (serial shift right or parallel). The shift mode is selected by the application of a logic 0 or logic 1 to mode input pin M.

Refer to figure 7. The control data and control gate inputs are applied in both the true and inverted states to SR flip-flop circuits U2A and U2B. The control word used as an example in figure 7 is control word II with subaddress bit 6 at logic 0 and subaddress bit 7 at logic 1.

The T-output (control data) of U2A is applied to the shift right serial (DS) input of U6. The T-output of U2B (control gate) is combined with the inverted output from U6-6 and applied to the mode control input (U6-M).

The F-output of U2B is combined with the control gate input and applied to the parallel strobe input (U6-S).

During a 36-bit monitor word period and the dialogic and 5-bit address period of the following control word, the mode control signal is held at logic 1, which holds U6 in the parallel shift state. Also, the logic 0 to 1 change of the control gate causes a logic 1 to 0 transition at the U6-S input and U6 shifts the parallel inputs (1, 7, 9, 12) to the outputs of U6 (6, 8, 11, 13). At the middle of bit period 6, the mode control signal changes to logic 0 and causes U6 to switch to the shift right state. When the clock signal goes to logic 0 at the end of bit period 7, U6-6 goes to logic 1 causing U6 to return to the parallel shift state where it remains until the control gate delayed by 1/2 bit ($CG_{1/2}$) from U2B-12 goes to logic 1. During the 2-bit shift right period, subaddress bits 6 and 7 are shifted to outputs 11 and 13 of U6 where they also remain for the same period. The subaddress bits are removed at the logic 0 to 1 change of the next control gate signal when the logic 1 to 0 strobe signal is applied to the parallel strobe input of U6. The subaddress outputs from U6 are applied to the word load logic circuits.

The output of the word gate timing circuit (U8B, U3A, U3B and U1E) that is applied to the word load logic circuits, is at logic 0 when the control gate is at logic 1. This logic 0 signal inhibits the word load logic circuits during this period by holding the outputs of U13A, U13B, and U13C at logic 1 (the enable signal is logic 0). Assuming control word II was sent, subaddress output from U6 (control word II) is applied to the word load logic circuits and the three outputs remain at logic 1 through bit period 31. At bit period 32 the control gate changes to logic 0 causing

the output of the word gate timing circuit to change to logic 1. The logic 1 timing signal causes the output of U13A to change to logic 0, the enable signal for the word II load output. The remaining two load gate outputs are unchanged. The logic 0 word II load gate is inverted and applied to the proper storage registers as a logic 1 load word II signal. The reason the load gate appears at the end of the control word period is to allow the entire control word to be loaded through the shift registers to the storage registers. The entire word is then shifted out when the load gate triggers the storage registers. The load pulse lasts 1/2 clock pulse and load storage is enabled by a logic 1.

The primary mode output signal is produced by the primary mode logic circuit and is at logic 0 only when both the control gate delayed by 1/2 bit ($CG_{1/2}$) and monitor gate inputs are at logic 0. The primary mode output is used for mode control (serial shift right or parallel shift) of the shift registers.

Power interrupt circuit U5 (refer to the schematic) provides a logic 1 power interrupt signal to the monitor circuits whenever a power interruption of more than 50 μs occurs. Depending upon processor programming, the line processor upon reception of a power interrupt signal may retransmit all three control words to prevent the possibility of a voltage transient being interpreted as control information.

The frequency load output is produced whenever a frequency control word (word I) is received. Under normal conditions, the load word I signal from U12C, except during the period when word I is being processed, is at logic 1, causing the frequency load output (U7A-11) to be logic 0. At the end of a word I control period, the word I load output from U12C changes to 0 and clocks U7A, causing a logic 1 frequency load output from U7A-11 for 1/2 bit period. This logic 1 is applied to frequency control card A14 to enable the frequency change circuits.

4.2.14.2 Shift and Storage Register Functions

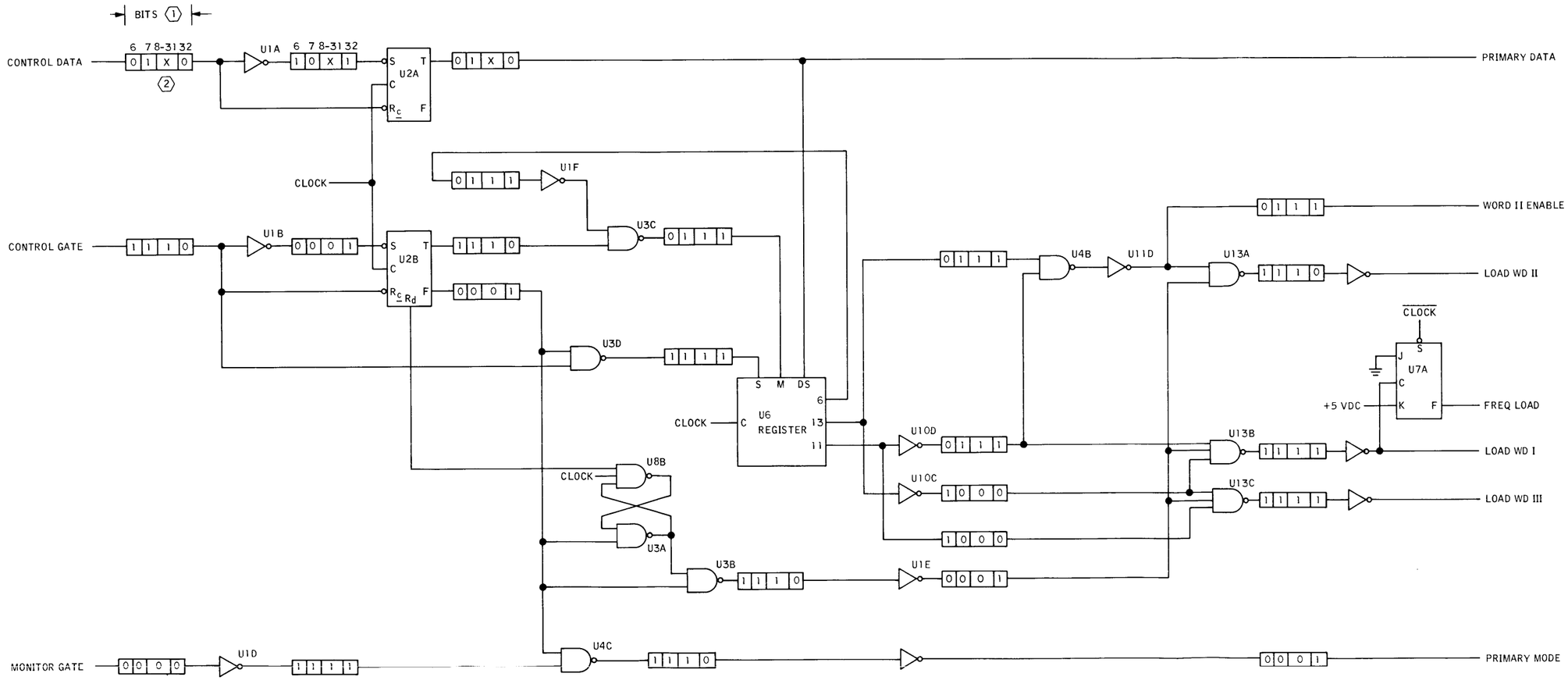
Figure 8 shows the typical operation of one shift register and two associated output storage registers. The operation of all these registers in the DCFE is identical. During a control word command period (bits 8 through 31) the primary mode signal is at logic 0 and is applied as the shift-right mode signal to U37-5. During this period, primary data (control information) is applied to data shift input U37-14 and is shifted serially from the four output lines of U37 to the inputs of U35 and U36. Shift register U37 is the first register to receive control information so all control bits in the control word must be shifted through it. At the end of bit period 31, the primary mode signal changes to logic 1, U37 then switches to the parallel shift mode and holds the last four bits of the control word (28 through 31) on the four parallel output lines. The previous bits have been shifted out on output number 4 (pin 6) of U37 to the shift right serial input (pin 14) of the succeeding shift registers (U33, U29, U25, U21, and U17).

Assume that frequency control information, control word I, is being processed. At bit period 31, the last four bits of frequency control information are on the four outputs of U37 and are held there because U37 is in the parallel shift mode. At bit period 32 the word I load gate input goes to logic 1 for 1/2 bit and is applied to the load input (pin 2) of storage register U36. The logic 1 load signal loads the frequency information onto the four outputs of U36 where it remains until the appearance of another logic 1 load gate. The other storage register has the same frequency information at the input, but the absence of the required load gate prevents the information from being loaded onto its output. These frequency outputs are applied, at this point, to all the applicable cards in the receiver and the cards then perform their respective functions.

Control bits 24 through 31 are loaded onto U34 and U38 for word III storage and generation. These registers operate the same as the registers mentioned above.

4.2.14.3 Monitor Word Processing

At the completion of a control word, monitor responses throughout the receiver are applied through the DCFE to the DCU for modulation. After control word I is processed by storage registers U16, U20, U24, U28, U32 and U36, the bcd frequency selected is monitored. Bcd information for 10 MHz-2 through 10 kHz-1 is applied to the B inputs of U18, U22, U26, and

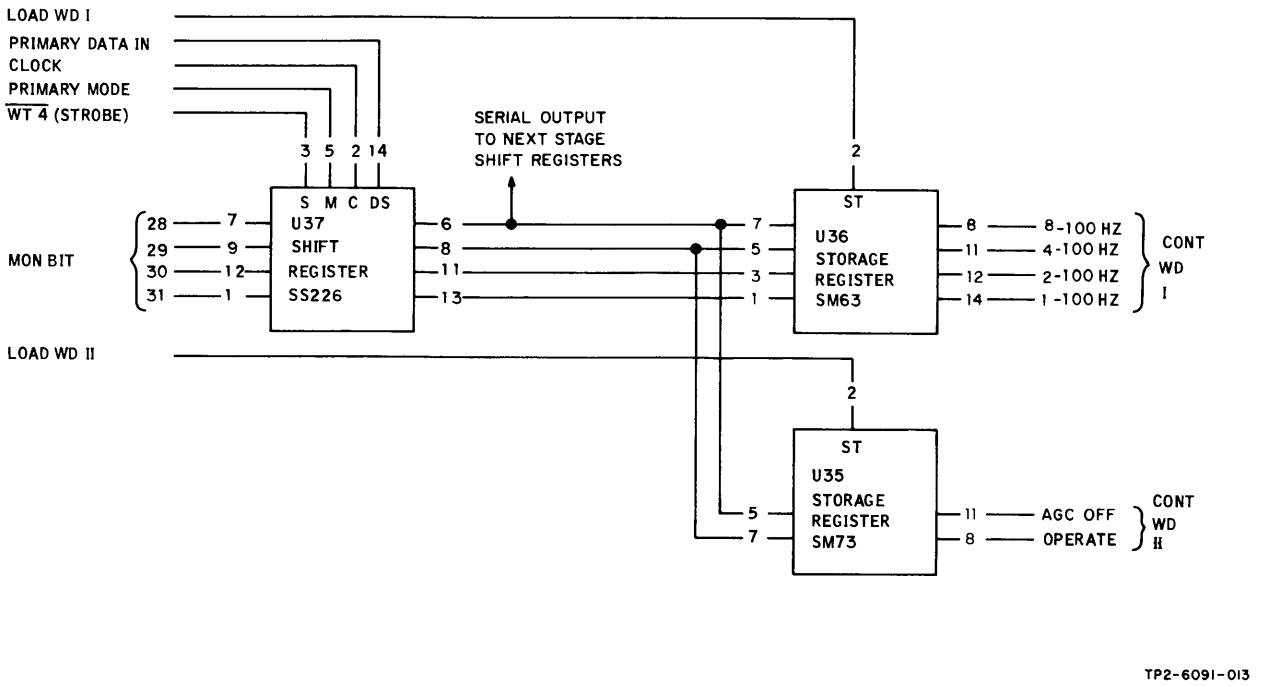


NOTES:

1. LOGIC STATE OF CONTROL WORD II SHOWN IN ALL LOGIC STRIPS.
2. X IN LOGIC STRIP DENOTES EITHER LOGIC 1 OR 0, NO EFFECT ON EXAMPLE.

TP3-0687-014

DCFE Control Word Routing, Functional Diagram
Figure 7



DCFE Shift Register/Storage Register Operation Functional Diagram
Figure 8

U30. Refer to figure 10. Bcd information for 1 kHz-8 through 100 Hz-1 is applied to U33 and U37. That portion applied to the 2-input, 4-bit multiplexers (U18, U22, U26, and U30) is sent directly to U17, U21, U25, and U29 because there is no word II enable signal at pin 9 of the multiplexers.

All the monitor bits are now at the parallel inputs of shift registers U17, U21, U25, U29, U33, and U37. The strobe (WT 4) input goes to logic 1 after bit 3 resulting in a logic 0 $\overline{\text{WT 4}}$ signal The $\overline{\text{WT 4}}$ strobe signal allows the inputs to be loaded onto the output lines of the registers. When the monitor gate goes to logic 1, the primary mode input changes to logic 0 (figure 9) and the registers switch to the serial shift right state. The monitor data is then serially shifted out of all the registers through U9 to the DCU.

Storage registers for the control words are unaffected during this operation due to the lack of proper control word gate signals. (Figure 9 also shows the timing relationship between monitor gate, control gate, control gate delayed 1/2 bit ($CG_{1/2}$), U6 enable and output signals, LD WD I, frequency load, and primary load signals.)

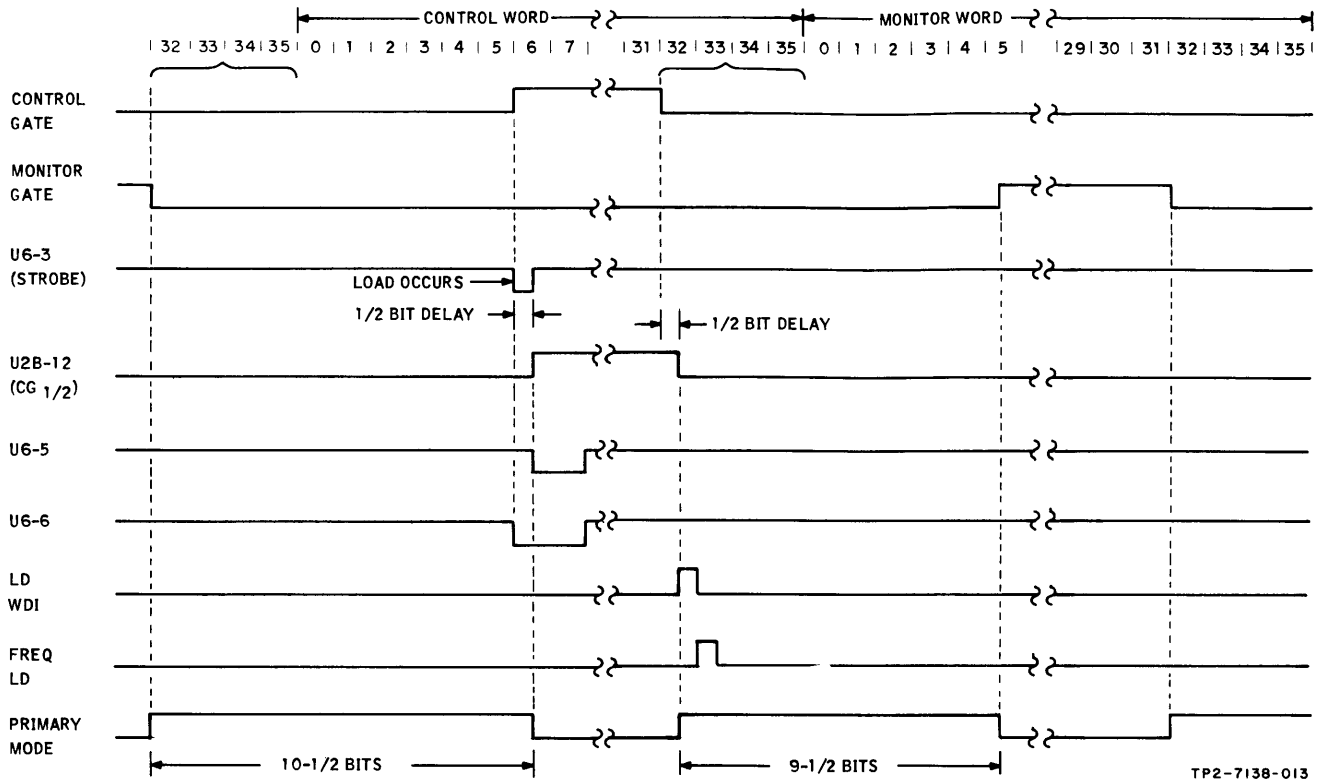
After control word II is processed, the same operation occurs, except that mode type monitor data is sent to the DCU. This mode monitor information is applied from various points in the receiver to the A inputs of multiplexers U18, U22, U26, and U30. This information is gated through the multiplexers upon the application of the word II enable signal. Word II enable occurs during control word II and during the following monitor word period (figure 7).

4.2.14.4 Local/Remote Switching

If the DCFE card is in place during local operation, control signals must pass from the front panel through the DCFE to the applicable cards. The local mode signals are applied to a diode matrix that applies them to the same output pins as the storage registers during remote control.

Relay K1 switches local/remote mode information to the pertinent cards. This relay is energized during remote control and is deenergized during local control.

Frequency tuning control information bypasses the DCFE during local operation and is applied directly to frequency control card A14. Frequency information, however, is monitored by



DCFE Enabling Signals, Timing Diagram
Figure 9

the DCFE in local operation and is transferred to the line processor by monitor words as described in 4.2.14.3.

4.2.15 DCU Card A9 (Optional)

4.2.15.1 DCU Card 793-9414-001

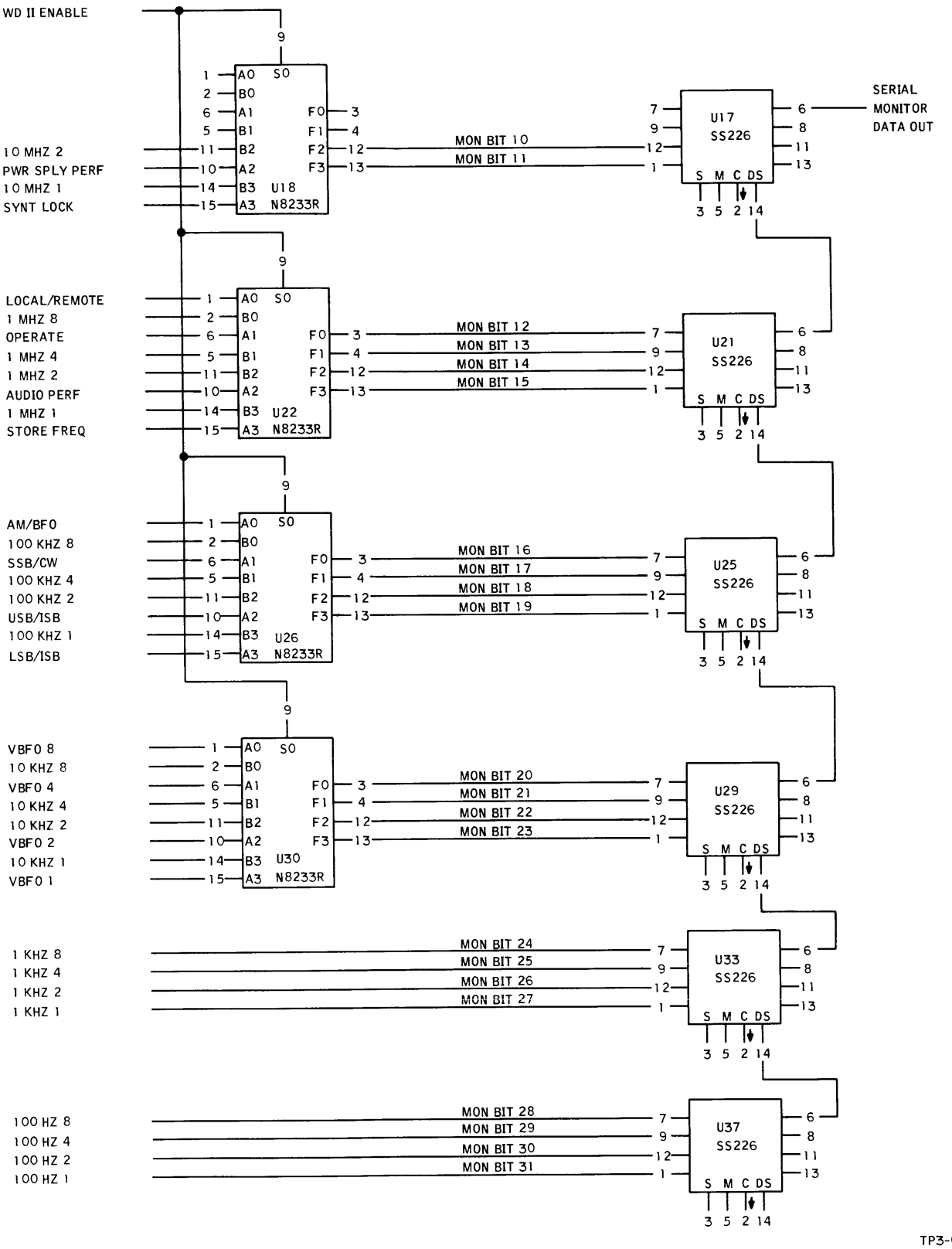
Refer to the schematic in the diagrams section. The DCU (device control unit) is a half-duplex device that accepts phase shifted sine-wave data from a digital processor on the control bus, converts it to digital data, and when properly addressed, permits DCFE card A8 to process the controlling portion (oper field) of this digital data. Alternatively, the DCU accepts digital data in serial form from the circuits of the DCFE, converts it to phase shifted sine-wave data, and transmits the sine-wave data to the DCU driver on the monitor bus. All operations within the DCU are synchronized by a sine-wave timing signal that is applied to the DCU on the carrier bus. The DCU converts this sine-wave signal to a digital bit clock signal. Figure 11 shows the three interface signals that are transmitted to and from the DCU.

4.2.15.2 DCU Control Bus to DCFE Data Transfer

Data from the digital processor is applied to the DCU on the control bus in the form of a biphase modulated sine wave. The control word formats are explained in the DCFE theory. The control word is routed through DCU interface amplifier U502 and is applied to U602 and U603. The half-wave rectified signal from U602 is filtered by integrator R12 and C7 to establish a dc reference level for comparator U603. The dc level is maintained at approximately one-half the peak value of the signal at the control bus terminals.

The output from U603 is a string of positive pulses that represents the demodulated serial data. (During the supervisory interval, the output from U603 is low.) The demodulated data from U603 passes through voltage shaper U404B and is then applied to the detector circuit.

The serial control information is detected by noting the relative position of the positive



DCFE Monitor Operation, Functional Diagram
Figure 10

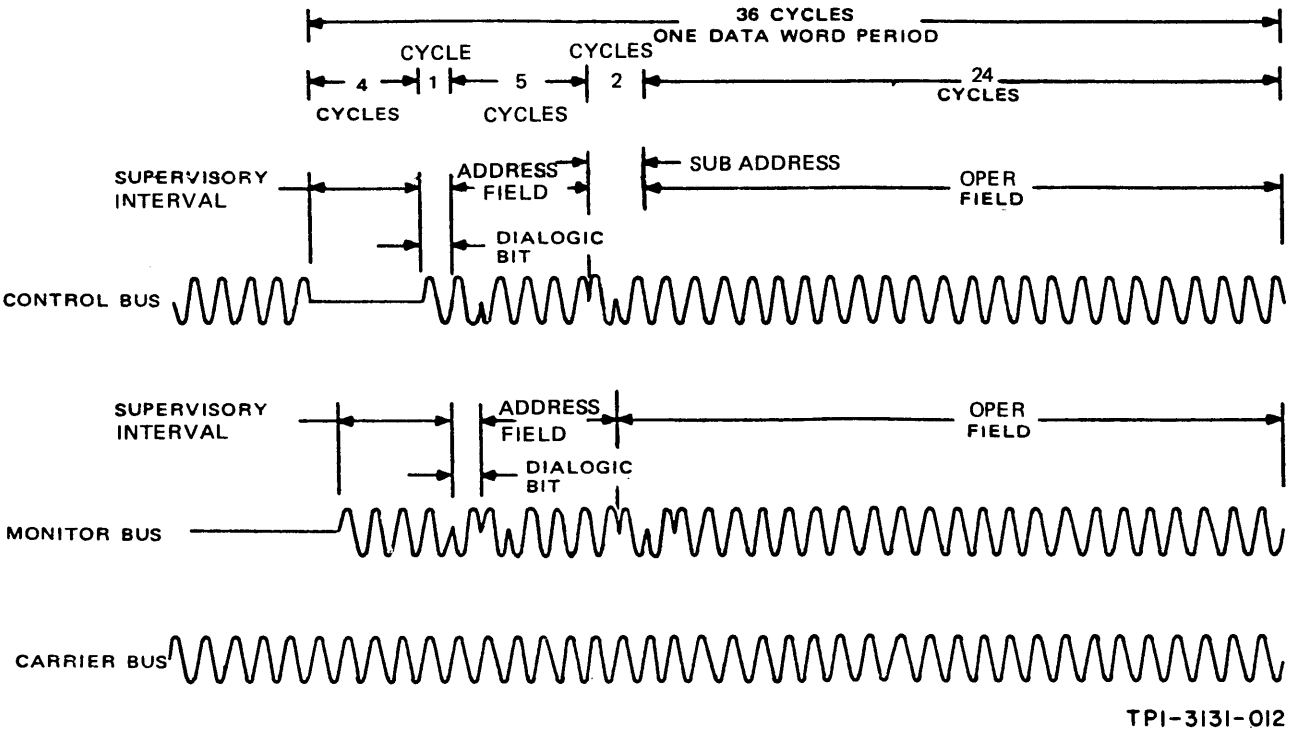
pulses from U404B during each bit cycle. The pulses are applied to flip-flops U402A and U402B and the positions of the pulses are decoded by U401A and U401D. U402A and U402B are clocked by the sampling clock and its inverse. (The sampling clock is shifted 90 degrees from the bit clock.)

If a positive pulse occurs early in a bit cycle, a logic 1 appears at U402B-Q and a logic 0 appears at U402A-Q. U401A detects this combination and applies a logic 1 to flip-flop U301B for data detection. Any other output combination from U402 results in a logic 0 output from U401A. The detected data is loaded into flip-flop U301B at the end of each bit clock period and U301B provides detected control data and detected control data outputs.

If no positive pulse occurs during a bit cycle, logic 0's appear at U402B-Q and U402A-Q. This combination is detected by U401D, which in turn applies a logic 1 to flip-flop U301A for sync detection. Any other output combination results in a logic 0 from U401D. Flip-flop U301A is loaded with the detected sync data at the end of each bit clock period and it provides the detected sync and detected sync outputs.

The carrier bus input is used to synchronize the timing of the entire operation between the DCU, and DCFE, and line processor. The carrier bus signal is routed through DCU interface amplifier U801, split, and applied to demodulator U802 and amplifier-filter U903. Demodulator U802 converts the carrier signal to a sampling clock for the data detector circuits (U402).

The automatic level control circuit (U903, Q1, and Q2) maintains the constant carrier bus output level (for clocks) despite the variation of the carrier input signal. The output of U903 is applied to differential switch Q2B. If the negative peak of the sine wave of U903 drops below the switching level of Q2A (determined by resistors R30 and R31), Q2A switches on and discharges C26. This reduces the voltage on the gate of Q1 (used as a voltage-controlled



DCU Interface Signals, Timing Diagram
Figure 11

resistor) and reduces the resistance from the junction of R26 and R28 to ground. This attenuates the signal level. If the U903 output is low, Q1 conducts less and more resistance to signal ground is developed, providing less attenuation to the signal.

The sine-wave clock signal is routed, as the modulator clock, to the monitor modulator circuit (U904 and associated circuits). The sine-wave clock is also converted to a square-wave bit clock signal by bit clock amplifier U803 and bit clock gate U404A. This bit clock signal clocks the time base counter, the data detector circuit (U301), and the output control circuits. It is also routed to the DCFE for synchronization purposes.

At this point, the 36 cycles of the control bus word have been operated on by the DCU as follows: the first four cycles (carrier off) were used to produce the det sync and $\overline{\text{det sync}}$ signals to maintain word synchronization, while the remaining 32 cycles of the control bus word have been converted to 32 control data bits. These 32 bits are routed to address recognition circuit U201B. A preselected address, controlled by strapping DCU address bit lines 1 through 5 to either a logic 1 or a logic 0, is applied to address code generator U103. The preselected DCU address from the address code generator is also applied, in serial form, to address recognition circuit U201B. When the address code contained in bits 1 through 5 of the control data word matches the preselected DCU address code, a logic 1 is applied by U101A to the control gate line. This logic 1 on the control gate line notifies the DCFE that a data word containing the correct address for this device (receiver) has been received by the DCU. At this time the DCFE circuits are enabled to process the remaining data bits (bits 6 through 31) that are present on the control data line.

4.2.15.3 Time Base and Output Control Circuits

The time base circuit generates all the timing signals required by the DCU. This circuit consists of an address code generator and a 36-counter circuit. The output control circuit controls the transfer of control and monitor information between the radio control unit, the DCU, and the DCFE. This circuit consists of sync detecting, address recognition, decoding, serial data gating, control and monitor gating, and modulator enabling circuits. Refer to figure 12 for the timing of the DCU.

The 36 counter circuit generates weight 1, 2, 4, 16, and 32 signals and $\overline{\text{weight 1, 2, 4,}}$ and $\overline{32}$ signals. The weight 32 and $\overline{\text{weight 32}}$ signals are applied to sync comparison circuit U201A and are compared by U201A to the det sync and $\overline{\text{det sync}}$ signals during the supervisory interval and during the dialogic and address bit intervals. If the det sync and weight 32 signals are not identical, the DCU is out of sync and flip-flop U102A applies a logic 0 set signal to counter flip-flops U203B, U203A, U204B, U204A, U304A, and U104. This set signal stops the counter and presets the counter flip-flops. When the weight 32 and det sync signals become identical, the set signal is removed and the counter resumes counting.

The last four flip-flops in the 36 counter (U204B, U204A, U304A, and U104) are disabled during the 4-bit supervisory interval. At the end of each 36-bit word period, the logic 0 output (supervisory interval) from U104-Q ($\overline{\text{weight 32}}$) is applied to the K input of counter flip-flop U204B. This logic 0 prevents any output change from U204B with the first 1 to 0 weight 2 transition on the clock input of U204B. The weight 2 clock pulse is also applied to the clock input of U104. The first 1 to 0 weight 2 transition changes the output states of U104, applying a logic 1 to the K input of U204B. The second 1 to 0 weight 2 transition then initiates the 32 count by clocking flip-flop U204B. This, in effect, expands the 32 counter to a 36 counter for use with the 36-bit word format.

The $\overline{\text{weight 32}}$ output is also applied to the set input of U304B. This set input to U304B is logic 0 during the supervisory interval, causing the output from U304B-Q to remain logic 1 during that period. At the end of the supervisory interval, the set input to U304B is changed to logic 1. The outputs from U304B do not change state, however, until the K input (WT 4) is logic 1 (the fourth bit after the end of the supervisory interval) and there is a logic 1 to 0 transition on the clock ($\overline{\text{WT 2}}$) input (the sixth bit after the end of the supervisory interval).

The logic 1 output from U304B-Q allows the bit clock signal to be routed through U304D. The bit clock signal is then applied to the clock input of flip-flop U102B during the first six bits after the supervisory interval (bits 0 through 5, the dialogic bit, and the address bits).

Address code generator U103 produces the dialogic bit (logic 0 in the DCU) and converts the strapped preset address (bit lines 1 through 5) to serial digital data. The dialogic bit and this serial coded address is applied to address recognition circuit U201B. (Strapping a DCU address bit line to ground produces a logic 0 in that bit position of the serial address format, and strapping an address bit line to +3 Vdc produces a logic 1 in that serial bit position.) Detected control data and $\overline{\text{detected control data}}$ signals are also applied to address recognition circuit U201B. If the address code contained in bits 1 through 5 of the control data signal matches the preset coded address from the address code generator, a logic 0 is applied to the K input of U102B. A logic 0 is then applied by U102B-$\overline{Q}$ to control gate U101A.

Six bits after the end of the supervisory interval, the outputs from U304B change states and a logic 0 appears at the U304B-Q output. This logic 0 prevents the bit clock signal from being routed through U403D to flip-flop U102B. If, during the dialogic bit period and the address bit period (bits 0 through 5), address recognition circuit U201B indicated that the DCU was correctly addressed, the logic 0 will remain at the input of control gate U101A.

The logic 0 output from U304B-Q is also applied to control gate U101A. Control gate U101A then applies a logic 1 to the control gate line. This logic 1 enables the proper DCFE circuits and the remaining control data bits (bits 6 through 31) are processed by the DCFE.

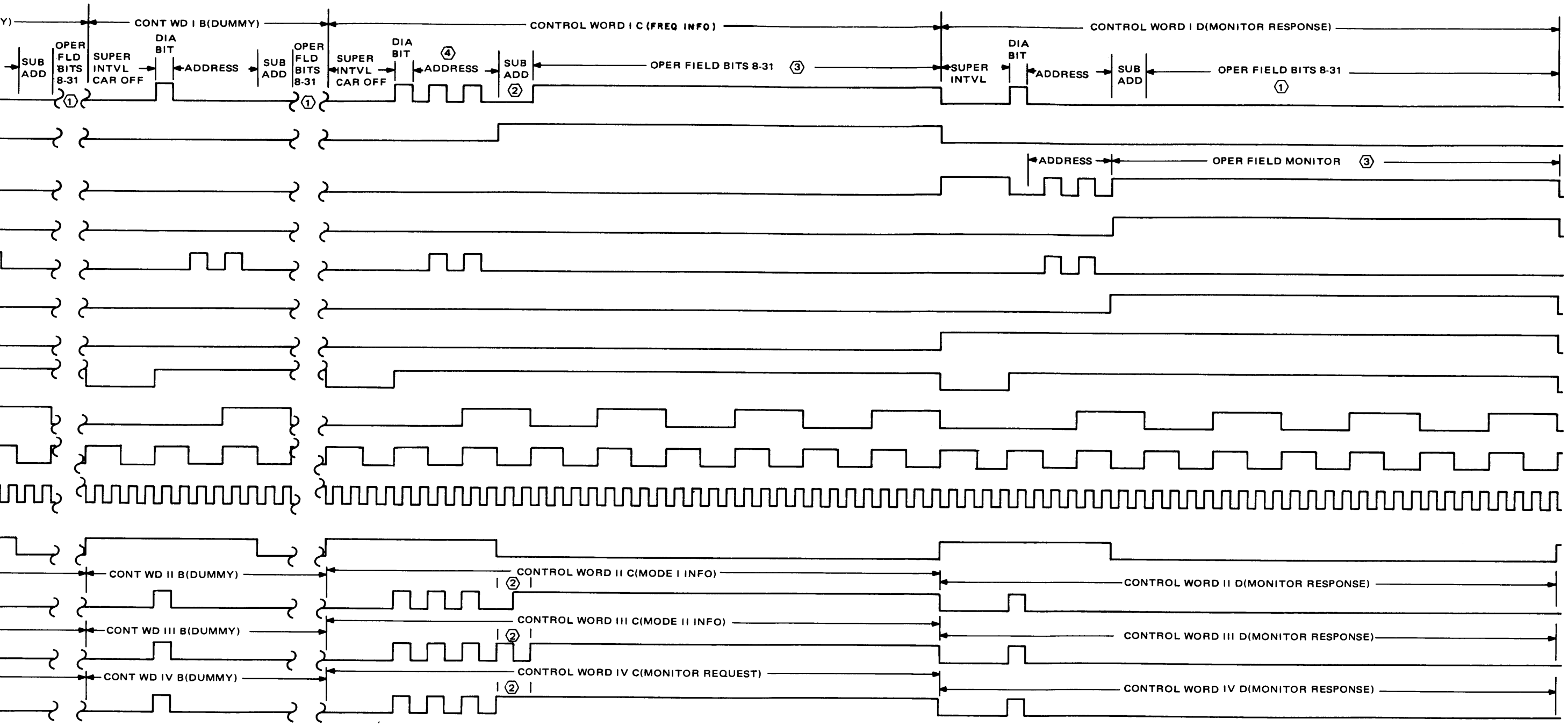
The logic 1 to 0 transition from U304B-Q is also applied to the clock input of U202A. This clock signal enables the transfer of information from flip-flop U102B to flip-flop U202B. If a correctly addressed control word was received by the DCU, a logic 1 is stored at U202A-13. The Q output of U202B, however, was preset to a logic 1 and the $\overline{Q}$ output was preset to a logic 0. These outputs will not change states until the next 1 to 0 transition of the $\overline{\text{weight 32}}$ output from U104-$\overline{Q}$ is applied to the U202B clock input. This transition occurs immediately at the end of the control word when the $\overline{\text{weight 32}}$ signal changes from 1 to 0, and flip-flop U202B is clocked. The outputs from U202B change states and a logic 0 is applied to the input of monitor gate U101D and a logic 1 is applied to modulator enable gates U403B and U403C.

The $\overline{\text{weight 32}}$ logic 0 is also applied to the set inputs of flip-flops U304B and U102B. At the end of the supervisory interval, $\overline{\text{weight 32}}$ changes to logic 1, removing the set inputs to these flip-flops. During the next six bits, U304B applies a logic 1 to monitor gate U101D. Gate U304B also allows the bit clock signal to clock U102B. Since there is no address on the detected control data and $\overline{\text{detected control data}}$ lines, address recognition circuit U201B applies a logic 1 to U102B, resulting in a logic 1 input to control gate U101A. This logic 1 disables the control gate.

The dialogic bit and serial address bits produced by address code generator U103 are applied to serial data gating circuit U303A. This serial address data is then routed through U303B for insertion into the monitor word.

Six bits after the supervisory interval, the output from U304B-Q changes to a logic 0, enabling monitor gate U101D. The monitor gate then applies a logic 1 to the monitor gate line. This logic 1 enables the monitor circuits in the DCFE, and the DCFE provides serial monitor data on the monitor data input to the DCU. This monitor data is gated through serial data gate U403A to U303B where it is combined with the serial address data to form a complete monitor word. Serial data gates U403B and U403C then pass the monitor word to the monitor modulation circuits.

The logic 1 to 0 transition from U304B-Q also clocks U202A and the information at the outputs of U102B is transferred by U202A to the inputs of U202B. A logic 1 is applied to the J input of U202B and a logic 0 is applied to the K input. When the next $\overline{\text{weight 32}}$ transition from logic 1 to 0 occurs, the outputs from U202B change states and a logic 1 is applied to the input of monitor gate U101D. This logic 1 disables the monitor gate. A logic 0 is applied by U202B-Q to serial data gates U403B and U403C. This logic 0 disables the serial data gates.



TOR RESPONSE CONTROL WORD OPER FIELD ALL 0'S.

CONT WD I = 00, CONT WD II = 01, CONT WD III = 10, CONT WD IV = 11.

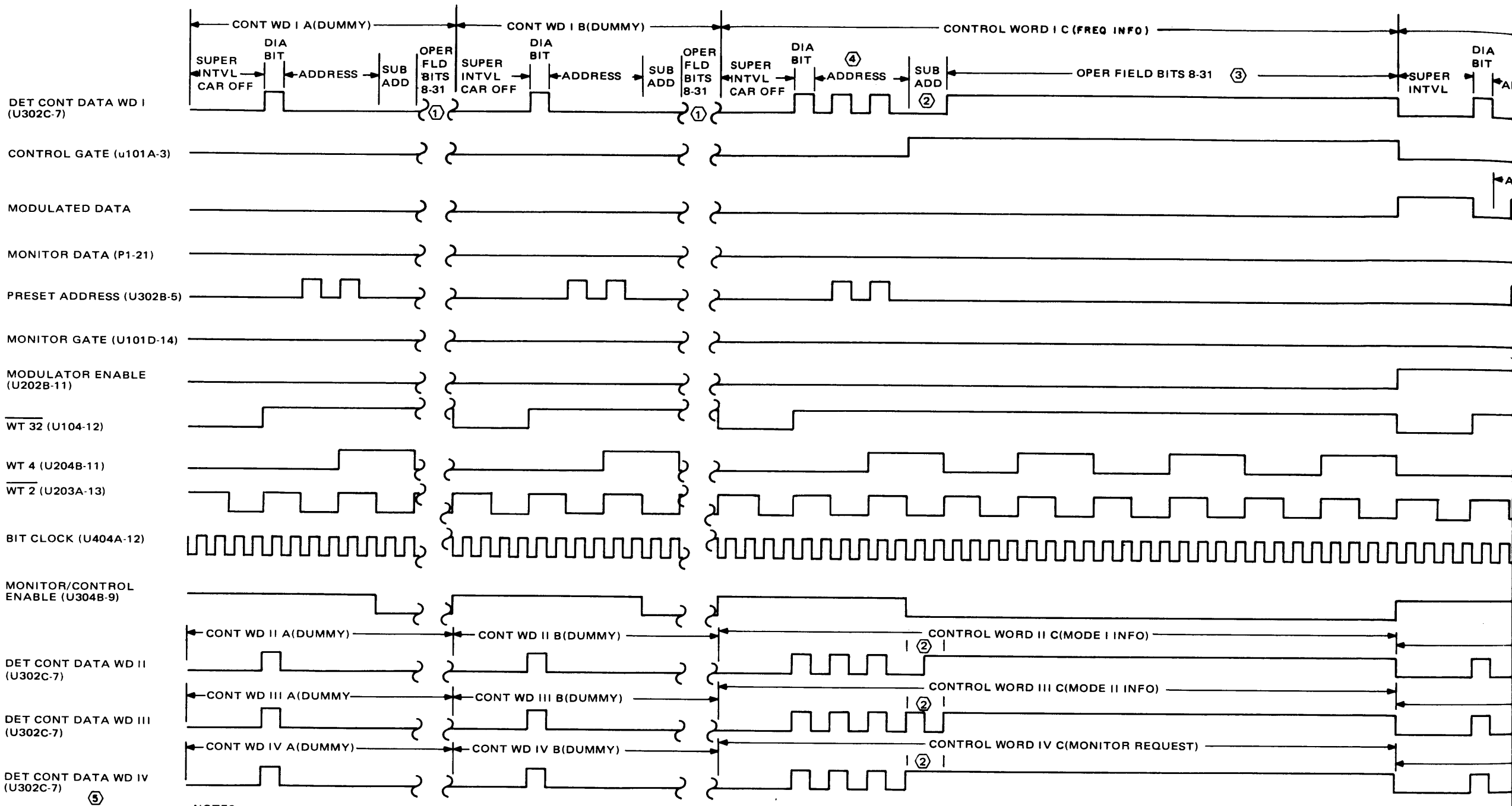
LL 1'S THIS EXAMPLE.

ET ADDRESS = 01010 THIS EXAMPLE.

OUSLY TRANSMITTED (AFTER WORDS I, II, AND III ARE ACCEPTED) TO
T STATUS.

TP2-5889-013

DCU Operation, Timing Diagram
Figure 12



NOTES:

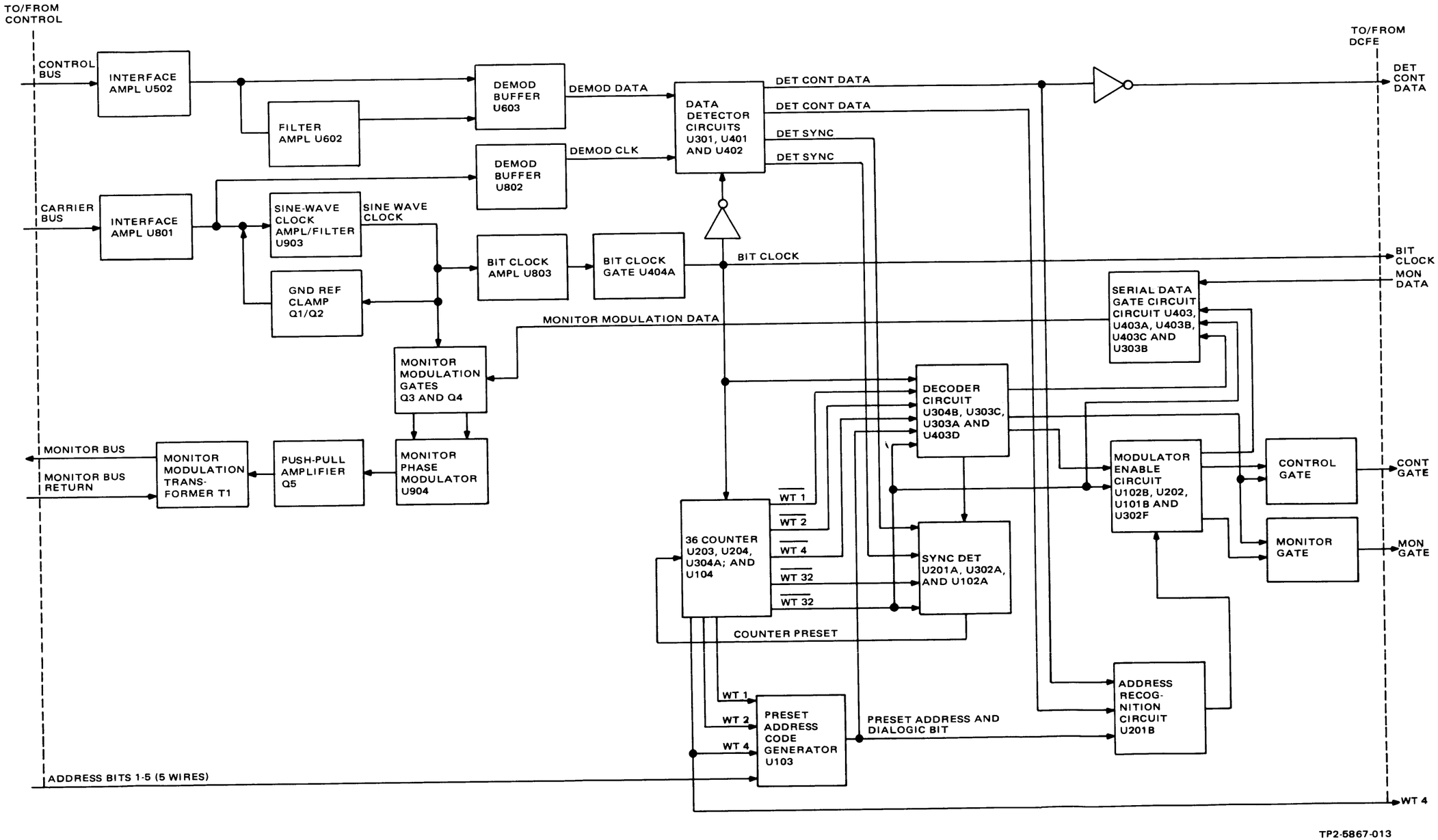
① DUMMY AND MONITOR RESPONSE CONTROL WORD OPER FIELD ALL 0'S.

② SUBADDRESS FOR CONT WD I = 00, CONT WD II = 01, CONT WD III = 10, CONT WD IV = 11.

③ OPER FIELD BITS ALL 1'S THIS EXAMPLE.

④ ADDRESS AND PRESET ADDRESS = 01010 THIS EXAMPLE.

⑤ CONT WD IV CONTINOUSLY TRANSMITTED (AFTER WORDS I, II, AND III ARE ACCEPTED) TO MONITOR EQUIPMENT STATUS.



DCU A9, Functional Diagram
Figure 13

When the weight 32 returns to logic 1, the DCU is ready to receive a new control word (or a repeat of the previous control word if the monitor response was incorrect). The DCU time base and output control circuits repeat the above sequencing each time a correctly addressed control word is received by the DCU.

4.2.15.4 Modulator Circuit

The serial monitor data from serial data gates U403B and U403C is routed through transistor gates Q3 and Q4 and is biphase modulated with the sine-wave clock by modulator amplifier U904. This biphase modulated data then passes through push-pull amplifier Q5 and is coupled through transformer T1 to the monitor bus. Table 9 in the DCFE theory lists the monitor word format.

4.2.15.5 DCU Card 624-5781-001

Refer to the schematic in the diagrams section. Functionally, this card is identical to the CPN 793-9414-001 version; however, thin-film circuits have been replaced with discrete flatpacks and components. For example, interface amplifier U502 is replaced by U61; filter amplifier U602 and demodulator buffer U603 are replaced by U51.

4.2.15.6 DCU Card 774-7842-001

Refer to the schematic in the diagrams section. Functionally the same as CPN 624-5781-001, except it operates at a much higher speed (carrier frequency). Discrete, flatpacks and components changed to accomplish high-speed operation, 76.8 kHz (bits per second).

4.2.16 TCU Card A9 (Optional)

Refer to figure 14 and to the schematic in the diagrams section. The TCU (teletypewriter converter unit) is a device that accepts standard ASCII TTY - coded control data at a 110-b/s data rate from a 514S-1 Remote Control Unit. The unit is addressable for multiunit use and control data can be either six characters of frequency data, eight characters of mode data, or characters for slewing the frequency of the receiver. Each character consists of eleven bits, a start bit, seven data bits, a parity bit, and two stop bits. The main functional elements of the TCU are the timing circuits, TTY character receiver, address control circuits, a down counter, DCFE interfacing circuits, error detector circuits, and scan control circuits.

4.2.16.1 Timing Circuits

The source of timing signals in the TCU is a free-running multivibrator containing transistors Q1 and Q2. Potentiometer R3 is adjusted for a 3521-Hz operating frequency. This master clock output is routed through pulse amplifier Q3 and inverters U103C and U103D to J-K flip-flop U112B, where it is divided by 2 to produce a 1760.5-Hz timing signal, WT1. J-K flip-flop U112A divides WT1 by 2, producing an 880.25-Hz timing signal, WT2. These three signals, master clock, WT1, and WT2, along with their complements, are distributed throughout the TCU for timing purposes.

Another main timing signal is the clock used in the TTY-character receiver portion of the TCU. This clock is enabled each time a start bit is received by the TCU. WT2F is applied through NOR gate U111D to the divide-by-8 portion of counter U101. The 110-Hz square-wave output from U101 The 110-Hz square-wave output from U101 is differentiated by C10 and R16 and routed through inverters U103A and U103F. The clock output from J103A is a short negative pulse, at a repetition rate of 100 p/s, and is used to clock the TTY-coded data bits into shift register U61.

4.2.16.2 TTY Character Receiver

TTY-coded characters are transmitted over the teletypewriter loop at 110 b/s using 20-mA mark/space signaling; that is, logic 1 is a 20-mA mark signal, and logic 0 is an absence of current or space signal. The TTY loop interface in the TCU is phototransistor U34 which conducts during mark signals and is cut off during space signals and produces an inverted output, DATAF.

Upon application of initial power to the board or the receipt of the stop bits at the end of a character, the TTY character receiver is enabled for the next character. DATAF, being a logic 0, is inverted by U103B and applied to J-K flip-flop U102A. The next time timing signal WT2 goes to logic 0, U102A is set. The T output, CHAR RCVR ENABLE (U102A-9), becomes logic 1 and removes the clear signal from shift register U61 and the reset signal from J-K flip-flop U73A. The F output (U102A-8) becomes logic 0, which enables the parity flip-flop and the divide-by-8 portions of counter U101 (paragraph 4.2.16.1).

During the start bit, DATAF becomes a logic 1. This signal is routed through U103B, U93D, and U93C and enables NOR gate U111D, which allows WT2F to be applied to the divide-by-8 portion of counter U101. DATAF is still a

logic 1 when the first clock pulse from U103A occurs, and is consequently clocked into shift register U61. This first clock also sets the F output of U73B to logic 0, which maintains the enabling of NOR gate U111D during the remaining bits of the character.

The next eight bits of the TTY character are clocked at a 110-b/s rate into shift register U61; and, simultaneously, routed through NOR gate U111A to the parity flip-flop portion of counter U101. The ninth clock pulse shifts the start bit, which has been shifted through shift register U61, into J-K flip-flop U73A. The strobe output of U73A, STB, enables NAND gate U13C, which is the parity check input to the error detection circuits. The other output of U73A, STBF, disables the divide-by-8 portion of U101 through NAND gate U93C and U111D, and prepares flip-flop U102A to be reset, through U111C, after the TTY-character has been processed. When U102A is reset, register U61 is cleared, U73A is reset, and all flip-flops in counter U101 are reset.

4.2.16.3 Address Processing

The first character to be received is the end of transmission (EOT) character. After being shifted into shift register U61, EOT is detected by the combinational logic of U71A, U83A, U81B, and U63C. The logic 0 output of U63C resets both U33A and U33B flip-flops and prepares them for the address character.

The next character to be received by the TCU is the address character. After being shifted into shift register U61, the four address bits are applied to exclusive OR gates U31A, U31B, U31C, and U31D. The other inputs to these exclusive OR gates are strapped to logic 1 or logic 0 to determine the address of the TCU. Because the address bits from U61 are inverted, the exclusive OR gates will have a logic 1 output only when the address character coincides with the strapped address. With a correct address received, the exclusive OR gate outputs are combined by NAND gates U32A and U32B, and cause NOR gate U42B to produce a logic 1 output, which is applied to the D input of flip-flop U33B. The clock signal to set U33B is produced by flip-flop U33A as STBF falls. If an incorrect address is received, U33B will not be set and will inhibit further characters from being processed. The address recognition circuit is normally disabled when a single radio is being controlled from a 514S-1 Remote Control Unit. This is accomplished by not strapping P1-26 (ALL CALL) to logic 0.

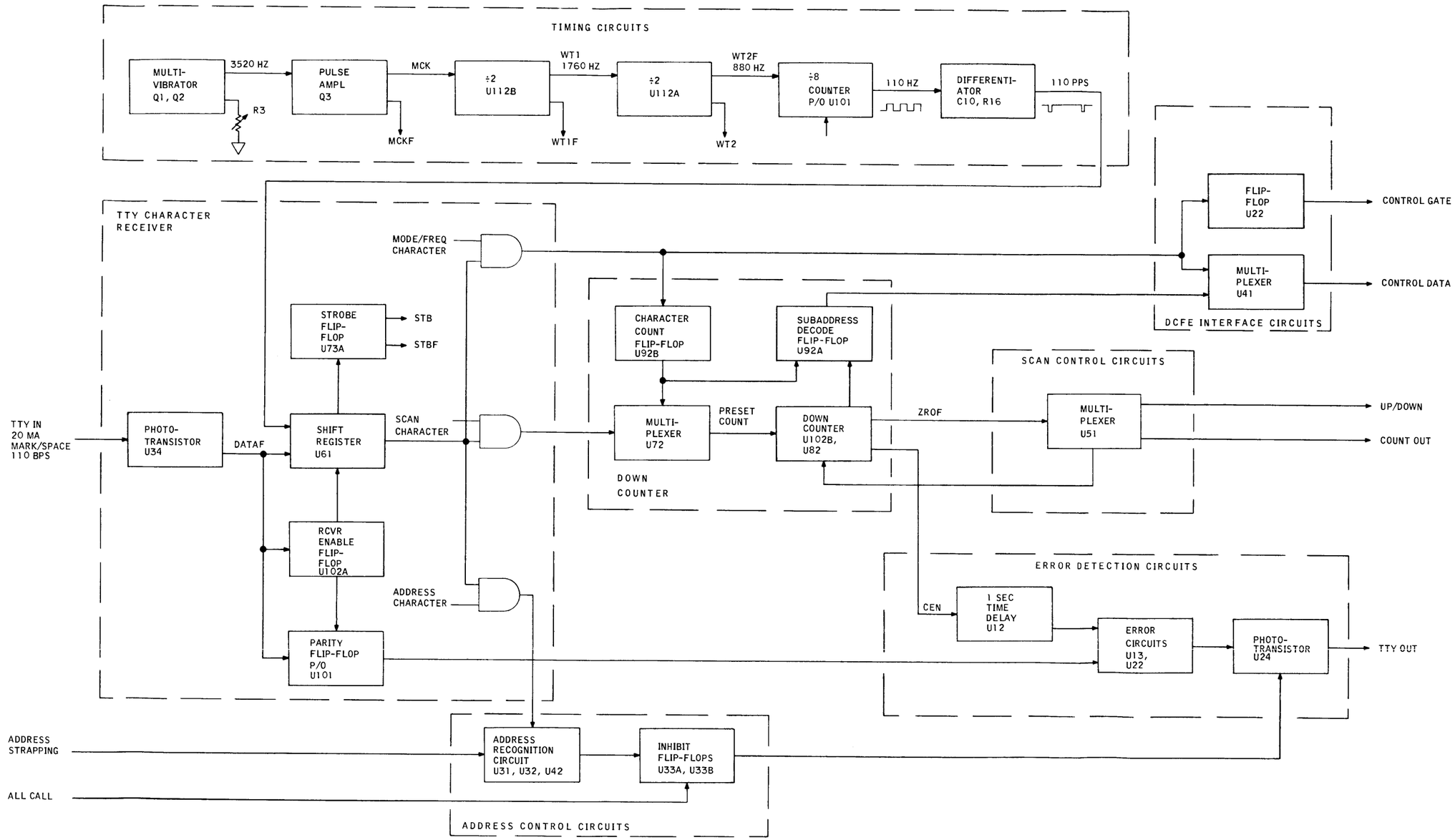
4.2.16.4 Mode and Frequency Words Processing

Mode and frequency data words are processed in almost the same manner; the main difference is that there are six characters of frequency data and eight characters of mode data.

For both types of words, a control gate and clock pulses must be applied to the DCFE. ASCII bit 7, out of shift register U61, is received as a logic 1 for these characters and is applied through NOR gate U62B and inverter U52E to NAND gate U13B. All other inputs to U13B are logic 1, which produces a logic 0 output that causes flip-flop circuit U22B and U22C to change to a state where the control gate, U22B-6, becomes logic 1. The control gate is applied to the DCFE and through U22D, which resets storage flip-flop U53B. STRF output, on U53B-12, becomes a logic 0 and disables AND gate U11D, which permits master clock MCKF to be applied through NOR gate U21B to the DCFE. Bits 5 and 7 of the first character for both words determine the subaddress used in the DCFE. Bit 7 is a logic 1 for both words to distinguish them from a scan word. Bit 5 distinguishes between a mode word (logic 0) and a frequency word (logic 1).

Bit 5 of the first mode/frequency character is used to preset counter U82 to either six (for frequency words) or eight (for mode words). Counter U82 counts each time a character is processed and determines when the appropriate number of characters for that type of word have been received. Bit 5, out of shift register U61, is applied to the D input of flip-flop U92B. If bit 5 is a logic 0, U92B remains unset; but if bit 5 is a logic 1, U92B is set. Both outputs of U92B are applied to the A inputs of multiplexer U72, and then to counter U82. Operation of counter U82 is described in paragraph 4.2.16.6.

The subaddress supplied to the DCFE is determined by the ASCII character received and how the character is processed by the subaddress decode circuit. The subaddress decode circuit consists of flip-flop U92A; NOR gates U81A, U81C, and U81D; NAND gates U91A and U91C; and inverter U52B. For frequency words, the



TP3-1436-014

TCU A9, Functional Diagram
Figure 14

subaddress is 00. For mode words, the subaddress is 10 for the first two characters, and 01 for the last six characters. The subaddress bits are applied to multiplexer U41 from inverter U52B and NAND gate U91C. These address bits are inverted and transferred to the DCFE by timing signals WT1 and WT2 during the period when the C input (U41-9) is a logic 0. After the subaddress has been shifted into DCFE, the first digit of mode/frequency data is shifted while the C input (U41-9) is a logic 1. Bits 1 through 4 contain the digit in the format (B1-B4) listed in tables 10 and 11. Subsequent characters are received and processed in a similar manner by the TCU.

Table 10. Control Data Format for Frequency Data.

ASCII BIT POSITION	CHARACTER 1	CHARACTER 2	CHARACTER 3	CHARACTER 4	CHARACTER 5	CHARACTER 6
B1	2^0 ┐ 10 MHz	2^0 ┐	2^0 ┐	2^0 ┐	2^0 ┐	2^0 ┐
B2	2^1 ┘	2^1	2^1	2^1	2^1	2^1
B3	0	2^2 1 MHz	2^2 100 kHz	2^2 10 kHz	2^2 1 kHz	2^2 100 Hz
B4	0	2^3 ┘	2^3 ┘	2^3 ┘	2^3 ┘	2^3 ┘
B5	1	1	1	1	1	1
B6	1	1	1	1	1	1
B7	0	0	0	0	0	0

1 = MARK SIGNAL
0 = SPACE SIGNAL

Table 11. Control Data Format for Mode Data.

ASCII BIT POSITION	CHARACTER 1	CHARACTER 2	CHARACTER 3	CHARACTER 4	CHARACTER 5	CHARACTER 6	CHARACTER 7	CHARACTER 8
B1	2^0 ┐	2^0 ┐	AM	VBFO	200 Hz	450 kHz BYPASS	10.35 MHz BYPASS	X
B2	2^1 VBFO	2^1 RF GAIN	NBFM	BFO	AGC SLOW	6 kHz	3 kHz	LOCAL
B3	2^2	2^2	0	ISB	0	LSB	1 kHz	OPERATE
B4	2^3 ┘	2^3 ┘	0	SSB/CW	INTER-POLATE	USB	500 Hz	AGC OFF
B5	0	0	0	0	0	0	0	0
B6	1	1	1	1	1	1	1	1
B7	0	0	0	0	0	0	0	0

1 = MARK SIGNAL
0 = SPACE SIGNAL

Thus, the control words specified in table 7 are transferred from the TCU to the DCFE in the following manner. For a frequency word, the first character processed contains data in bit positions 6 through 11 of control word I; the second character covers bits 12 through 15; the third covers 16 through 19; etc. For a mode word, the first character processed contains data in bit positions 6, 7, and 24 through 27 of control word III; the second character covers bits 28 through 31; the third covers bits 6 through 11 of control word II; the fourth covers bits 12 through 15; the fifth covers 16 through 19; etc.

4.2.16.5 Scan Word Processing

A scan word can be one character or a string of characters; with each character representing a number from 1 to 31. Scan characters will be received continuously as long as the 514S-1 manual tuning control is rotated.

The seven data bits of each scan character are identified in table 12. Bits 1 through 5 contain the number of scan pulses, up to a maximum of 31 pulses, that are required to slew the 651S-1 to the desired frequency. Each pulse represents a frequency change of 100 Hz. Bit 6 identifies whether the frequency should be slewed up or down. Bit 7 identifies a scan character and not a mode/frequency character.

Bits 1 through 5, from shift register U61, are applied to a 5-bit counter consisting of J-K flip-flop U102B and counter U82. Bit 1 is applied to U102B through NAND gate U43B and inverter U52D. Bits 2 through 5 are routed through multiplexer U72 and applied to counter U82. Detail operation of counter U82 is described in paragraph 4.2.16.6.

Multiplexer U51 has multiple applications: a scan control portion and a portion used with counter U82. In general, the input applied to S0 (U51-9) controls its operation. When S0 is a logic 0, the B0 through B3 inputs appear on the F0 through F3 outputs. When S0 is a logic 1, the A0 through A3 inputs appear inverted on the F0 through F3 outputs.

In the scan mode, bit 7 is a logic 1 and is applied to S0 input of multiplexer U51; thus enabling the A inputs. Timing signal WT1F is applied through NOR gate U42C to A2 input of U51. The inverted timing signal appearing at

Table 12. Control Data Format for Slew Control Data.

ASCII BIT POSITION	SLEW DOWN	SLEW UP
B1	2^0 ┐	2^0 ┐
B2	2^1 │	2^1 │
B3	2^2 COUNTDOWN VALUE	2^2 COUNT UP VALUE
B4	2^3 │	2^3 │
B5	2^4 ┘	2^4 ┘
B6	1	0
B7	1	1

1 = MARK SIGNAL
0 = SPACE SIGNAL

F2 output advances counter U82, and is routed back to the A0 input of U51. The inverted output, F0 on U51-3, is the count out signal used to slew the 651S-1. Bit 6, which determines slew up or slew down, is routed from shift register U61 through inverter U52C to the A1 input of U51. Both the up/down out signal at F1 (U51-4) and the count out signal are applied to frequency control card A14. When all the slew pulses have been processed, as determined by counter U82, the scan operation is complete.

4.2.16.6 Down Counter Operation

The down counter is a 5-bit counter that consists of J-K flip-flop U102B, counter U82, and various combinational logic elements. The down counter has two purposes: first, to count the number of characters received for mode/frequency words; and secondly, to count the number of slew pulses received in a scan word.

In a quiescent state, down counter contains a 1 in all five flip-flops (U102B, and four in U82). The five outputs are combined in NAND gate U71B, which causes ZROF (U71B-8) to be a logic 0. ZROF is inverted by U103 and applied to NOR gate U83C. The logic 0 from U83C is applied to the J-K inputs of U102B and inhibit any further counting.

Counter U82 is preset to other counts by multiplexer U72, which has two different applications. In general, the input applied to S0

(U72-9) controls its operation. When S0 is a logic 0, the B0 through B3 inputs appear on the F0 through F3 outputs. When S0 is a logic 1, the A0 through A3 inputs appear inverted on the F0 through F3 outputs. S0 is a logic 0 during scan characters, and permits the number of scan pulses stored in shift register U61 to be transferred to counter U82. During mode/frequency words, S0 is a logic 1 and permits the number of characters to be received (6 for frequency, 8 for mode) to be transferred from flip-flop U92B to counter U82.

The output of counter U82 and U102 is always the 1's complement of the number desired. For example, if a count of 8 (01000) is desired, its 1's complement, 23 (10111), is set into counter U82 and U102. Then, when the counter had advanced 8 counts to 31, the counter reaches its quiescent state.

The 1's complement of the desired count is determined by multiplexer U72 and U102, with the output of U72 being transferred to counter U82 by load signal LODF from a flip-flop circuit consisting of U63B and U63C. This load signal is produced by strobe signal STB at the end of the first mode/frequency/scan character.

With the counter preset, its counting action is now enabled through NAND gate U71B, inverter U103, and NOR gate U83C. Additionally, logic gates U81A, U91A, and U91D set flip-flop U92A to enable the subaddress decode circuit if a mode/frequency word is received. The output from U92A is routed through both NOR gates U81C and U81D to NOR gate U83C, which maintains the counter enable.

Once the counter has been preset and enabled, the counter can be advanced to its quiescent state by clocking flip-flop U102B, through NAND gate U93B, in one of three ways. The fastest clocking occurs when an error has been detected; then 3521-Hz MCK signal is routed through NAND gate U93A to U93B. The second fastest way is during a scan character; then 1760.5-Hz WT1F is routed through NOR gate U42C and multiplexer U51 to U93B. The slowest clocking of counter U82 occurs during mode/frequency word processing. During this time, the strobe signal STB, at the rate of 10 Hz, is routed through NOR gates U62A and U21A, NAND gate U63A, and multiplexer U51 to U93B.

4.2.16.7 Error Detection Circuit

Two types of errors can be detected: parity and word execution time. NAND gate U13C checks for odd parity during strobe signal STB; and delay AND gate U12A checks for mode/frequency word completion within 1 second. If either fault occurs, flip-flop circuit U22A and U13B is set so that phototransistor U24 is cut off; thus producing a space or error (no current) condition on the teletypewriter loop. The no-fault condition is maintained when the TCU has not been addressed in the all-call mode.

4.2.17 Auto Scan Card A9 (Optional)

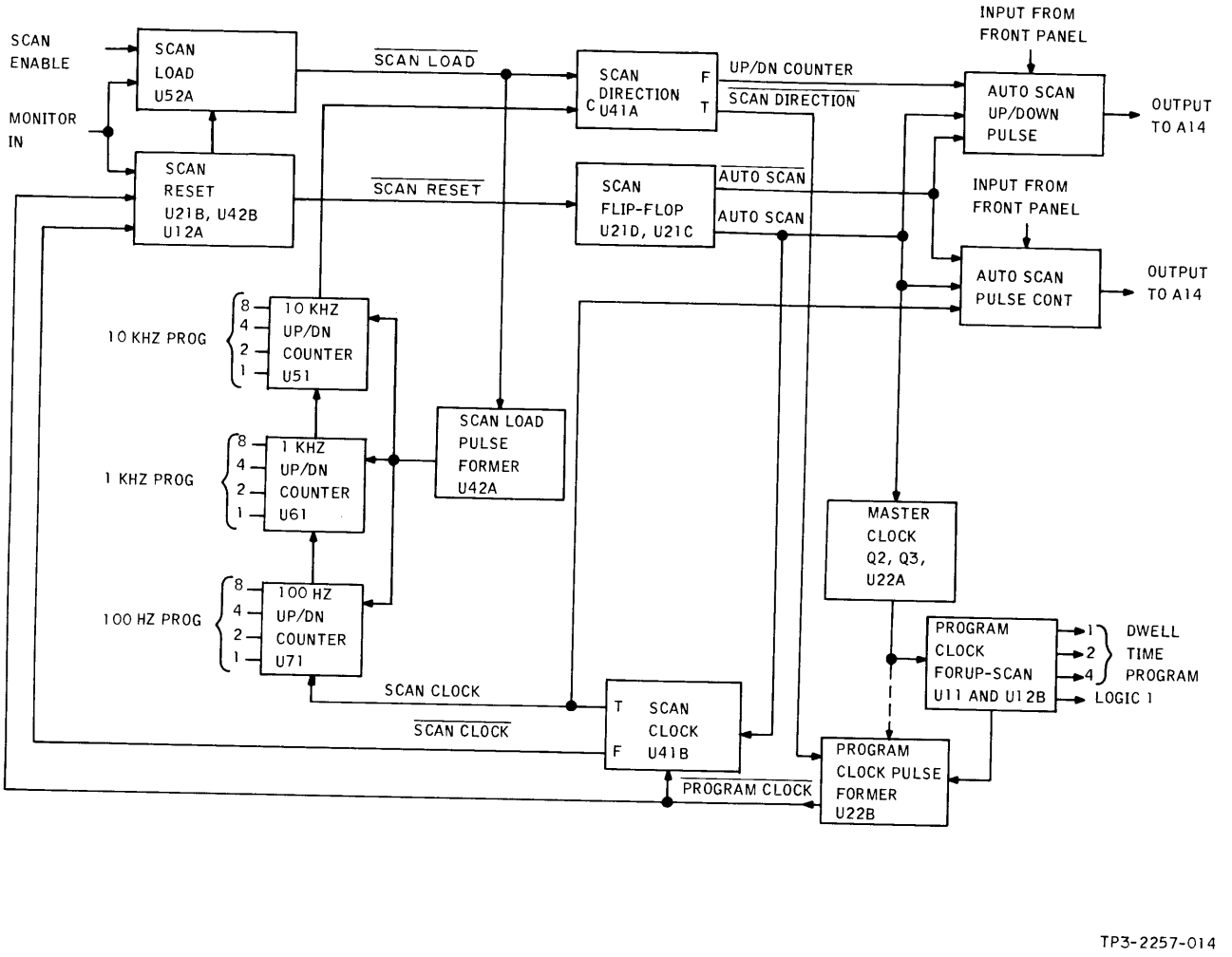
Refer to figure 15 and the schematic in the diagrams section. Auto scan card A9 receives frequency information from the front panel frequency controls and converts it into frequency scan data and applies this data to frequency control card A14. The two outputs are a frequency-count pulse (clock pulse) and a scan-up (logic 1) or scan-down (logic 0) signal.

4.2.17.1 Timing Signals (Figure 16)

The source of timing signals in the auto scan card is an RC controlled master clock consisting of Q2, Q3, and their associated components. A logic 0 input (scan-up operation) is inverted by U62E and applied to the base of Q2. When Q2 is enabled, C4 is added to the master clock RC network and the clock output pulse rate decreases. The master clock pulse is divided (countdown) by U11, the division ratio is determined by the dwell-time programmed into U11. The output of U11 is the program clock signal. The program clock pulses are divided (by 2) by JK flip-flop U41B to produce the scan clock signal.

4.2.17.2 Scan-up Operation

An enable signal (logic 1) from the REMOTE/LOCAL switch on the front panel enables Q1. The logic 0 on the collector of Q1 is routed through inverters U62B and U62C to JK flip-flop U52A. The F-output (pin 4) of U52A goes to logic 0 and is applied back to K (pin 6) to reset U52A. However, the short logic 0 trigger is applied to the R-input (pin 12) of U41A and also through pulse former U42A to reset up/down counters U51, U61, and U71 to their programmed initial state.

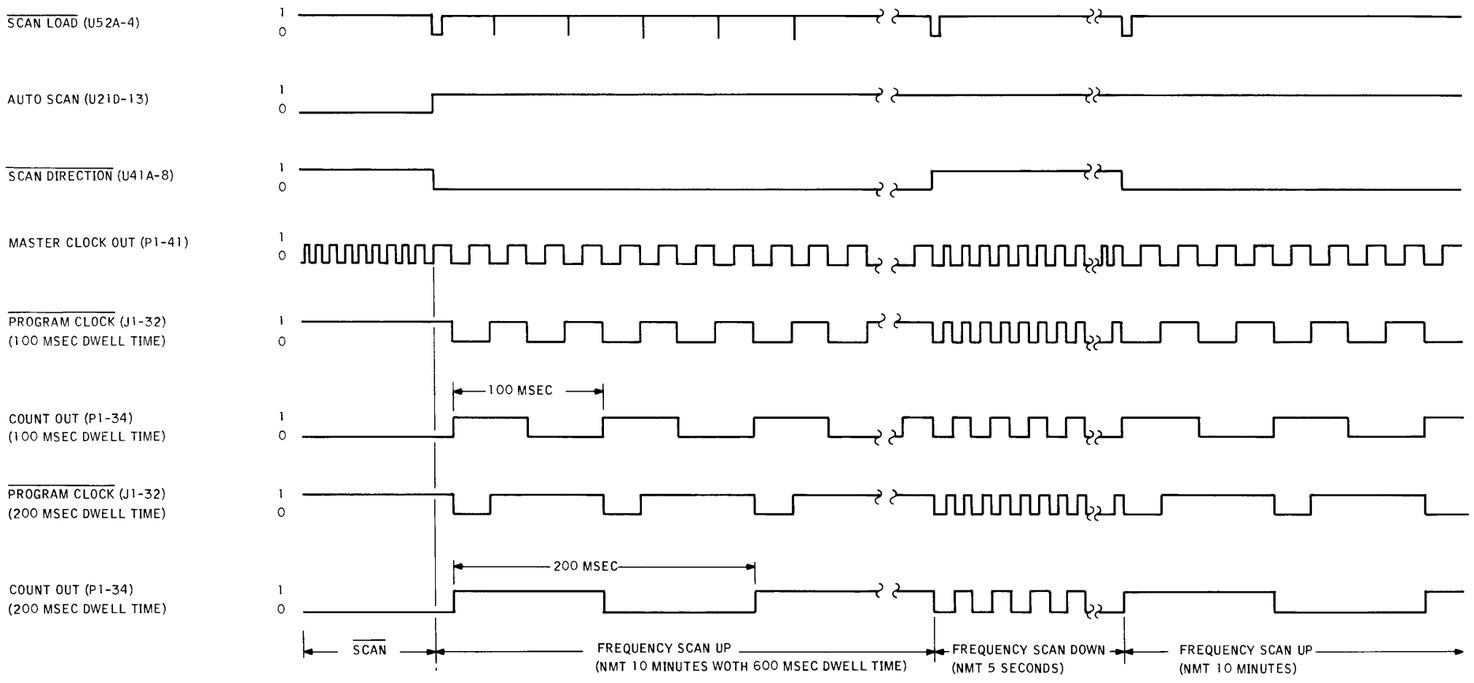


Auto Scan Control Card A9, Functional Diagram
Figure 15

The F-output of U41A (logic 1) is applied to the input of U31D in the auto scan circuit; the T-output (logic 0) is inverted by U62E and applied to the master clock circuit. The output of the master clock is inverted by U62D routed through pulse former U22A and applied to the program clock circuit U11 and U12B. The output of U12B (program clock) is routed through pulse former U22B and applied to the scan clock flip-flop U41B; simultaneously it is applied to U12A in the scan reset circuit.

The auto scan flip-flop U21D and U21C receives enabling signals (logic 1) from U12A and U24B (scan reset). The auto scan signal (logic 1) from U21D-13 is applied to U41B (scan clock) and to U31D and U32C in the auto scan circuit. The $\overline{\text{auto scan}}$ signal (logic 0) from U21C-10 is applied to U31C and U31B in the auto scan circuit.

The T-output (scan clock) of U41B triggers the frequency up/down counter U71 and is simultaneously



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Auto Scan Control Card A9, Timing Diagram
Figure 16

applied to U32C in the auto scan circuit; the F-output (scan clock) is applied to U21B in the scan reset circuit.

During scan-up operation (maximum of 10 minutes), the scan direction output (P1-31) will remain a logic 1; the frequency count output (P1-34) will be a clock pulse with the pulse rate determined by the scan clock which in turn is determined by the dwell time programmed into U11. This condition remains until up/down counters U71, U61, and U51 count up through the programmed frequency scan range. At the upper frequency limit, U51-12 applies a logic 1 to scan direction flip-flop U41A. This will cause U41A to reverse outputs and start the scan-down sequence.

4.2.17.3 Scan-Down Operation

A logic 1 from U51-12 causes U41A to reverse outputs, the F-output (logic 0) is routed through U31D and U31A to P1-31. A logic 0 output will cause frequency control card A14 to start scanning down in frequency. The T-output (logic 1) of U41A is inverted through U62E and applied as a disabling signal to Q2. With Q2 disabled, C4 is removed from the RC network of the master clock; shorter RC time will increase the master clock output pulse rate. Simultaneously the scan direction signal (logic 0) is applied to the input of U21A. The output of the master clock is routed through U62D and U22A and applied to the input of U21A. U21A is enabled bypassing dwell-time program clock U11 and U12B. The clock output of U22B will be the same pulse rate as the master clock.

The program clock signal is applied to U12A and in turn resets the scan-load flip-flop U52A, applying the scan-load trigger (logic 0) through U42A to reset the frequency up/down counters U51, U61, and U71 to their initial state. The F-output of U41B (scan clock) enables the scan-reset circuit (U21B and U42B) that in turn resets the auto scan flip-flop (U21D and U21C). Simultaneously, the T-output (scan clock) of U41B will start U71, U61, and U51 counting down. However, the scan down rate will be much faster than the scan-up rate. When the lower frequency limit is reached, a logic signal from U51-12 will cause U41A to reserve and the up-scan cycle will be repeated.

During scan-down operation (maximum of 5 seconds), the scan direction output (P1-31) will remain a logic 0; the frequency count output (P1-34) will be a clock pulse. However, the pulse rate will be much faster than in the scan-up sequence.

5. DIFFERENCE DATA

5.1 Configurations of 651S-1/1A

The following list explains the unique features of each configuration of the 651S-1/1A by part number identifier. Refer to table 1 for the complement of cards included in each.

5.1.1 651S-1

a. 522-4836-004: features local control; standard operating modes of FM, AM, SSB, and CW; bandwidths of 370 (offset 2 kHz) and 500 Hz, and 1.1 (offset 2 kHz), 2.7, 3, 6, and 16 kHz; has audio squelch.
b. 522-4836-102: features local control; standard operating modes of FM, AM, SSB, and CW; and bandwidths of 500 Hz and 2.7, 6, and 16 kHz.
c. 522-4836-103: features Collins 3-pair serial digital remote control, and standard operating modes and bandwidths listed in step b.
d. 522-4836-104: features local control; standard operating modes and bandwidths listed in step b, plus 370-Hz (offset 2 kHz) (narrow shift radioteletypewriter, NSRT) and 1.1-kHz (offset 2 kHz) (wide shift radioteletypewriter, WSRT) bandwidths.
e. 522-4836-106: features local control; standard operating modes and bandwidths listed in step b; plus independent sideband (ISB).
f. 522-4836-107: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; ISB; and bandwidths of 0.2, 1.0, and 3.0 kHz.
g. 522-4836-108: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; and bandwidths of 0.2, 1.0, and 3.0 kHz.
h. 522-4836-110: features local control; standard operating modes and bandwidths listed in step b; ISB; and bandwidths of 0.2, 1.0, and 3.0 kHz.
i. 522-4836-111: features local control; standard operating modes and bandwidths listed in step b; and bandwidths of 0.2, 1.0, and 3.0 kHz.

j. 522-4836-113: features Collins 3-pair serial digital remote control and standard operating modes and bandwidths listed in step b; bandwidths of 0.2, 1.0, and 3.0 kHz; and a special modification for fast external rf gain.
k. 522-4836-120: features local control, standard operating modes and bandwidths listed in step b; has vlf converter.
l. 522-4836-121: features local control; standard operating modes and bandwidths listed in step b; bandwidths of 0.2, 1.0, and 3.0 kHz; has audio squelch.
m. 522-4836-122: features local control; standard operating modes and bandwidths listed in step b; ISB; bandwidths of 0.2, 1.0, and 3.0 kHz; has audio squelch.
n. 522-4836-123: features remote teletypewriter coded control and standard operating modes and bandwidths listed in step b.
o. 522-4836-124: features local control; standard operating modes and bandwidths listed in step b; has audio squelch.
p. 522-4836-125: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; has audio squelch.
q. 522-4826-126: features local control; standard operating modes and bandwidths; has a special gray front panel.
r. 522-4836-128: features Collins 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 1.1, 2, 2.7, 3, 4, 6, and 16 kHz.
s. 522-4836-129: features Collins 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 500 Hz and 1.1, 2.7, 3, 6, and 16 Hz.
t. 522-4836-131: features 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz and 1, 2.7, 3, 6, and 16 kHz plus ISB; has audio squelch.
u. 522-4836-132: features local control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz; and vlf converter.
v. 522-4836-133: features local control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz plus ISB; has vlf converter.
w. 522-4836-134: features local control; standard operating modes listed in step b; bandwidth of 370 Hz (offset +2 kHz) (narrow shift radioteletypewriter, NSRT) 500 Hz, 1.1 kHz, (offset +2 kHz) (wide shift radioteletypewriter, WSRT) and 2.7, 3, 6, and 16 kHz.
x. 522-4836-135: features 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz and 1, 2.7, 3, 6, and 16 kHz plus ISB; has vlf converter and audio squelch.
y. 522-4836-152: features local control; standard operating modes AM, SSB, and CW; bandwidths of 2.7, 6, and 16 kHz.
z. 522-4836-153: functionally identical to part no -152, except has DCFE and DCU cards for remote control.
aa. 522-4836-154: features local control standard operating modes listed in step y; bandwidths of 320 Hz (NSRT) (offset +2 kHz), 500 Hz, 1.1 kHz (WSRT), (offset +2 kHz), and 2.7, 3, 6, and 16 kHz.
ab. 522-4836-156: functionally identical to part no -152, except has ISB card for ISB operation.
ac. 522-4836-173: functionally identical to part no -152, except has audio squelch.
ad. 522-4836-179: functionally identical to part no -153, except has a hi-speed DCU card (76.8 kHz).
ae. 522-4836-180: features local control; standard operating modes listed in step y; bandwidths of 500 Hz, 1.1 kHz (offset +2.55 kHz, WBTY), and 2.7, 3, 6, and 16 kHz.
af. 522-4836-181: functionally identical to part no -180, except has ISB card added.
ag. 522-4836-182: functionally identical to part no -180 except has vlf converter added.
ah. 522-4836-183: features Collins 3-pair serial digital remote control; standard operating modes listed in step y plus FM; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz; has FM detector, keep alive voltage, preselector control, and fast rf gain control.
ai. 522-4836-184: features Collins 3-pair serial digital remote control; standard operating modes listed in step y; bandwidths of 1.1 kHz (offset +2 kHz) and 2, 2.7, 3, 4, 6, and 16 kHz; has VBFO of 455.5 kHz and fast gain control.

5.1.2 651S-1A

622-1062-001: features local control; standard operating modes of AM, SSB, and CW; bandwidths of 370 Hz (narrow shift radioteletypewriter, NSRT), 500 Hz, 1.1 kHz (wide shift radioteletypewriter, WSRT), and 2.7, 3, 6, and 16 kHz; has audio squelch.

5.2 Card Configurations

The following list explains the unique features of the various cards, identified by part number.

a. A2, 778-2948-003 (old version): 600-ohm center tapped, 8-ohm speaker and 600-ohm headphone outputs; vbfo circuits that produce bfo variations in SSB of ±60 Hz in 10-Hz steps, and in CW of ±900 Hz.
b. A2, 778-2948-003 (current production model): functionally same as old version except operational amplifier U2, T1, and T2 in vbfo replaced with transistor Q6 and associated components.
c. A2, 778-2948-002: same as part no -003 old version, except with squelch operating an audio signal-to-noise ratio.
d. A2, 778-2948-004: same as part no -003 current production model, except with squelch operating on audio signal-to-noise ratio.
e. A2, 778-2948-005: same as part no -003 current production model, except Y1 is changed to 4.4555 MHz.
f. A4, 778-2951-001: standard if amplifier card with FM.
g. A4, 778-2951-003: same as part no -001, except with special modification for fast external rf gain.
h. A4, 778-2951-004: same as part no -001, except no FM.
i. A5A1, 797-3571-001, -006, -007, -010, -016, -012: only difference between each status is the bandwidth filters, see schematic in the diagrams section.
j. A5A2, 797-3585-002, -003, -004, -010, -011, -012: only difference between each status is the bandwidth filters, see schematic in the diagrams section.
k. A6, 790-1048-010, -021: the -010 differs from standard rf module A6 part no -008, and -021 differs from standard rf module part no -020 by providing a vlf up-converter for frequencies less than 560 kHz.
l. A6, 790-1048-008, -020: standard rf modules functionally the same, part no -020 is the current production model.
m. A7, 778-2928-003: standard 10-band decoder/driver card.
n. A7, 608-9087-001: standard 3-band decoder/driver card replaces the 778-2928-003 card.
o. A7, 608-9121-001: same as 608-9087-001, except has bcd outputs used with a 635U-2 external preselector.
p. A9, (DCU) 793-9414-001/624-5781-001/774-7342-001: functionally the same with discrete flatpacks on 624-5781-001 and 774-7843-001 replacing thin-film circuits on 793-9414-001. The 774-7843-001 is a hi-speed version (76.8 kHz/bits per second).
q. A10, 793-9334-001, -002: standard synthesizer divides cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
r. A10, 793-9334-006: differs from standard synthesizer divider card part no -002 by providing injection frequencies 9.9 MHz above the incoming signals, for vlf operation below 560 kHz.
s. A11, 793-9333-001, -002: standard synthesizer reference cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
t. A12, 793-9332-001, -002: standard synthesizer mixer cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
u. A13, 793-9331-002, -003: standard synthesizer vco cards functionally the same, with discrete flatpacks on part no -003 replacing thin-film circuits on part no -002.